GUJARAT TECHNOLOGICAL UNIVERSITY (GTU)

Competency-focused Outcome-based Green Curriculum-2021 (COGC-2021)
Semester-VI

Course Title: VLSI
(Course Code: 4361102)

Diploma programme in which this course is offered	Semester in which offered
Electronics & Communication	6th

1. RATIONALE

Digital integrated circuits are integral part of electronic equipment/gadgets starting from small toys to complex computer systems including personal digital assistants, mobile phones and Multimedia agents. This course will enable the students to acquire the basic skills to develop codes for VLSI circuits through **Verilog** programming and the fabrication process. This course will also enable them to use FPGA and ASIC chips for design and development of various applications. Thus this course is an advance but very useful course for electronic engineers.

2. COMPETENCY

The course content should be taught and implemented with the aim to develop required skills in the students so that they are able to acquire following competency:

- **Develop Verilog programs for VLSI based electronic systems**

3. COURSE OUTCOMES (COs)

The theory should be taught and practical should be undertaken in such a manner that students are able to acquire required learning outcomes in cognitive, psychomotor and affective domains to demonstrate the following course outcomes:

I. Describe working of MOSFET system
II. Maintain MOS inverters
III. Maintain MOS circuits
IV. Describe fabrication process for MOS
V. Develop VERILOG Programs for combinational and sequential circuits

4. TEACHING AND EXAMINATION SCHEME

Teaching Scheme (In Hours)			Total Credits (L+T+P/2)	Examination Scheme				
				Theory Marks		Practical Marks		Total Marks
L	T	P	C	CA	ESE	CA	ESE	
3	0	2	4	30*	70	25	25	150

(*):Out of 30 marks under the theory CA, 10 marks are for assessment of the micro-project to facilitate integration of COs and the remaining 20 marks is the average of 2 tests to be taken during the semester for assessing the attainment of the cognitive domain UOs required for the attainment of the COs.

Legends: L-Lecture; **T** – Tutorial/Teacher Guided Theory Practice; **P** -Practical; **C** – Credit, **CA** - Continuous Assessment; **ESE** -End Semester Examination.

5. SUGGESTED PRACTICAL EXERCISES:

The following practical outcomes (PrOs) are the subcomponents of the Course Outcomes (Cos). Some of the PrOs marked '*' are compulsory, as they are crucial for that particular CO at the 'Precision Level' of Dave's Taxonomy related to 'Psychomotor Domain'.

Sr. No.	Practical Outcomes (PrOs)	Unit No.	Approx. Hrs. Required
1.	Identify Verilog modules and coding styles	**V**	**2**
2.	Simulate the Basic logic gates using Verilog	**III, V**	**2**
3.	Simulate universal gates using Verilog	**III**	**2**
4.	Simulate XOR and XNOR using Verilog	**III**	**2**
5.	Simulate Half adder using Verilog	**III**	**2**
6.	Simulate full adder using half adder in Verilog	**III**	**2**
7.	Simulate four bit adder using Verilog	**III**	**2**
8.	Simulate 4 x1 multiplexer using Verilog	**III**	**2**
9.	Simulate 1 x 4 de-mux using Verilog	**III**	**2**
10.	Simulate 3 : 8 decoder using Verilog	**III**	**2**
11.	Simulate 8 : 3 encoder using Verilog	**III**	**2**
12.	Simulate Parity generator and checker using Verilog	**III**	**2**
13.	Simulate flip-flops (SR , D, T, JK) using Verilog	**III**	**2**
14.	Simulate 4 bit Up counter using Verilog	**III**	**2**
15.	Simulate 4 bit shift register using Verilog	**III**	**2**
16.	Verify digital circuits by implementing testbench for it in Verilog	**III, V**	**2**
17.	Hardware implementation of above programs	**III, IV, V**	**2**
			28 Hrs

Note

(a) More Practical Exercises can be designed and offered by the respective course teacher to develop the industry relevant skills/outcomes to match the COs. The above table is only a suggestive list.

(b) The following are some sample 'Process' and 'Product' related skills (more may be added/deleted depending on the course) that occur in the above listed Practical Exercises of this course required which are embedded in the COs and ultimately the competency.

Sr. No.	Sample Performance Indicators for the PrOs	Weightage in %
1.	Understand the basic concept, modules, and models of Verilog design	**20**
2.	Code in Verilog for digital circuits	**30**
3.	Use appropriate modeling style for a circuit	**20**
4.	Test device implementation	**30**
Total Hours (perform any of the practical exercises for a total of minimum 28 hours from above list depending upon the availability of resources so that skills matching with the most of the outcomes in the every unit is included)		**100**

6. MAJOR EQUIPMENT/ INSTRUMENTS REQUIRED

This major equipment with broad specifications for the PrOs is a guide to procure them by the administrators to use in uniformity of practical's in all institutions across the state.

Sr.No.	Equipment Name with Broad Specifications	PrO. No.
i.	Computer System	ALL
ii.	VLSI Trainer Kits	ALL
iii.	Verilog Simulator Software	ALL

Software/Learning Websites

i. QUARTUS-II-ALTERA EVAL VERSION
ii. ModelSim® HDL simulator for use by students in their academic coursework.
iii. ISE Simulator
iv. https://www.edaplayground.com/
v. https://vlab.amrita.edu/?sub=3&brch=66&sim=532&cnt=867

7. AFFECTIVE DOMAIN OUTCOMES

The following ***sample*** Affective Domain Outcomes (ADOs) are embedded in many of the above-mentioned COs and PrOs. More could be added to fulfill the development of this competency.

a) Work as a leader/a team member.
b) Follow ethical practices.

The ADOs are best developed through the laboratory/field-based exercises. Moreover, the level of achievement of the ADOs according to Krathwohl's 'Affective Domain Taxonomy' should gradually increase as planned below:

i. 'Valuing Level' in 1st
ii. year'Organization Level' in 2nd
iii year.'Characterization Level' in 3rd
. year.

8. UNDERPINNING THEORY:

Only the major Underpinning Theory is formulated as higher level UOs of *Revised Bloom's taxonomy* in order development of the COs and competency is not missed out by the students and teachers. If required, more such higher level UOs could be included by the course teacher to focus on attainment of COs and competency.

Unit	**Unit Outcomes (UOs)** **(4 to 6 UOs at Application and above level)**		**Topics and Sub-topics**
Unit – I. MOS Transistor	1a	Explain Energy and Diagram and Structure of MOS	1.1 MOS structure
	1b	Explain effect of external bias on two terminal MOS device with energy band diagram	1.2 MOS system under external bias
	1c	Explain Formation of channel with different symbols of MOSFET.	1.3 Structure and operation of MOSFET transistor
	1d	Explain gradual channel approximation	1.4 MOSFET current-voltage Characteristics
	1e	Explain the needs of scaling	1.5 Full-Voltage Scaling, Constant-Voltage Scaling.
	1f	Advance MOSFET technologies	1.6 Structure of High-K, FINFET, metal gate technology
Unit– II MOS Inverters	**2a**	Explain the working of MOS Inverter	2.1 MOS Inverter : concept and working
	2b	Explain operation of resistive load inverter without mathematical derivation	2.2 Resistive load Inverter
	2c	Describe inverter circuit with saturated and Linear Enhancement type load	2.3 Inverter with n-type MOSFET Load, Enhancement load NMOS
	2d	Explain Depletion type load and compare enhancement load NMOS with Depletion Load NMOS.	2.4 Depletion Load NMOS
	2e	Explain CMOS Inverter with different Operating Modes of nMOS and pMOS transistor.	2.5 CMOS Inverter: Circuit operation and description

Unit– III MOS Circuits	**3a**	Explain two input NAND and NOR Gate with depletion NMOS load	3.1 Combinational MOS Logic Circuits.
	3b	Explain Two input NAND and NOR Gate using CMOS logic.	3.2 CMOS logic circuits
	3c	Differentiate AOI and OAI Logic	3.3 Complex logic circuit
	3d	Design simple XOR function.	
	3e	Describe the working of SR latch circuit.	3.4 Sequential MOS circuit
	3f	Distinguish Clocked latch and Flip-Flop circuit.	
Unit– IV Fabrication of MOSFET	4a	Overview of VLSI design methodology and VLSI design flow	4.1 VLSI design flow, Y chart
	4b	Design hierarchy, Concept of regularity, Modularity, and Locality	4.2 Define terms: hierarchy, regularity, modularity, locality
	4c	Fabrication Process flow: Basic steps, CMOS n-Well Process	4.3 Lithography, Etching, Deposition, Oxidation, Ion implantation, Diffusion
Unit-V Introduction to VERILOG	5a	Verilog: HDL fundamentals, simulation, and test-bench design	5.1 Module definition and Stimulus generation
	5b	Develop Verilog Programs related to basic logic gates	5.2 Logic gate implementation in Verilog
	5c	Develop Verilog Programs related to Fundamental Arithmetic operations.	5.3 Verilog for adder and subtractor circuits
	5d	Develop Verilog Programs related to Combinational circuits.	5.4 Combinational circuits: Multiplexer , Demultiplexer, Decoder and Encoder 5.5 Parity Generator and parity checker.
	5e	Develop Verilog Programs related to Sequential circuits.	5.6 Basic Sequential circuits : SR latch, D F/F, T F/F, JK F/F 5.7 Parallel input Parallel output Shift Register, Up Counter, Down Counter

9. SUGGESTED SPECIFICATION TABLE FOR QUESTIONPAPER DESIGN:

Unit	Unit Title		Distribution of Theory Marks

		Teaching Hours	R Level	U Level	A Level	Total Marks
1	MOS Transistor	**8**	2	6	6	**14**
2	MOS Inverters	**6**	2	4	6	**12**
3	MOS Circuit	**10**	5	5	8	**18**
4	Fabrication of MOSFET	**6**	6	2	2	**10**
5	Introduction to VERILOG	**12**	3	5	8	**16**
Total		**42**	**18**	**22**	**30**	**70**

Legends: *R=Remember, U=Understand, A=Apply and above (Revised Bloom's taxonomy)*

10. SUGGESTED STUDENT ACTIVITIES

Other than the laboratory learning, following are the suggested student-related ***co-curricular*** activities which can be undertaken to accelerate the attainment of the various outcomes in this course: Students should conduct following activities in group and prepare reports of each activity.

i. Prepare chart to represent the CMOS design process
ii. Prepare chart to represent the technological advancements in CMOS technology starting from transistors to current technology
iii. Project- Build a small ASIC for your Home /Community.
iv. Prepare chart showing the types of FPGA technology
v. List out methods used in industries for each step used in CMOS design process.

11. SUGGESTED SPECIAL INSTRUCTIONAL STRATEGIES

These are sample strategies, which the teacher can use to accelerate the attainment of the various outcomes in this course:

i. Show Video/ Animation film explaining VLSI Design which are available on internet.
ii. Arrange expert lecture on VHDL programming for real life applications.
iii. Massive open online courses (MOOCs) may be used to teach various topics/sub topics.
iv. Guide students for using latest Technical Magazine
v. Visit industries where equipment/gadgets using VLSI are being manufactured/ assembled.
vii. Guide student(s) in undertaking micro-projects.

12. SUGGESTED PROJECT LIST

Only one micro-project is planned to be undertaken by a student that needs to be assigned to him/her in the beginning of the semester. In the first four semesters, the micro-project is group-based. However, in the fifth and sixth semesters, it should be preferably be ***individually*** undertaken to build up the skill and confidence in every student to become problem solver so that s/he contributes to the projects of the industry. In special situations where groups have to be formed for micro-projects, the number of students in the group should ***not exceed three.***

The micro-project could be industry application based, internet-based, workshop-based, laboratory-based or field-based. Each micro-project should encompass two or more COs which are in fact, an integration of PrOs, UOs and ADOs. Each student will have to maintain dated work diary consisting of individual contribution in the project work and give a seminar presentation of it before submission. The total duration of the micro-project should not be less than ***16 (sixteen) student engagement hours*** during the course. The student ought to submit micro-project by the end of the semester to develop the industry-oriented COs.

A suggestive list of micro-projects is given here. This has to match the competency and the COs. Similar micro-projects could be added by the concerned course teacher.

MICRO PROJECT 1: Prepare following Items.

1. Prepare graph showing relationship between feature size, number of transistors and year.

MICRO PROJECT 2: Design Application oriented basic Project using FPGA.

1. Design and Implement LED flasher circuit.
2. Design and Implement circuit for relay-based operation using switch.
3. Design and Implement Room Temperature Monitor/Controller System.
4. Design and Implement Water Level Indicator/controller circuit

MICRO PROJECT 3: Prepare following Items.

1. Prepare chart indicating the types of etching processes used with its application.
2. Prepare chart indicating the deposition processes with its application.
3. Prepare a survey report on the types of transistors used in memory elements.
4. Prepare a survey report on requirements of clean room and its classification

13. SUGGESTED LEARNING RESOURCES

Sr. No.	Title of Book	Author	Publication
1.	CMOS DIGITAL INTEGRATED CIRCUITS	Sung Mo Kang	TMH
2.	Introduction to VLSI Circuits and Systems.	Uyemura J.P.	WILEY INDIA PVT. LTD.
3.	VLSI DESIGN	Das Debaprasad	OXFORD
4.	VLSI DESIGN Theory and Practice	Vij Vikrant,Er. Syal Nidhi	LAXMI PUBLICATIONS PVT. LTD.
5.	CMOS Circuit Design, Layout, and Simulation	Baker, Li, Boyce	Wiley
6.	Verilog HDL : A Guide to Digital design and Synthesis	Samir Palnitkar	SunSoft Press

7.	A Verilog HDL Primer.	Bhasker (J).	Bsp Professional Books

14. SOFTWARE/LEARNING WEBSITES

1 https://eda.sw.siemens.com/en-US/
2. https://nptel.ac.in/courses/117106092
3. https://nptel.ac.in/courses/103106075
4. https://archive.nptel.ac.in/courses/113/106/113106062/

15. PO-COMPETENCY-CO MAPPING:

Program Outcomes (POs):

1. **Basic & Discipline specific knowledge**: An apply knowledge of basic mathematics, science and engineering fundamentals and engineering specialization to solve the engineering problems.
2. **Problem Analysis:** Identify and analyze well defined engineering problems using codified standard methods.
3. **Design/ Development of Solution:** Design solutions for well-defined technical problems and assist with the design of systems, components or processes to meet specified needs.
4. **Engineering Tools, Experimentation and Testing:** Apply modern engineering tools and relevant technique to conduct standard tests and measurements.
5. **Engineering practices for Society, Environment and sustainability**: Apply relevant technology in context of Society, sustainability, environment and ethical practices.
6. **Project Management**: Use engineering management principles individually, as a team member or a leader to manage projects and effectively communicate about welldefined engineering activities.
7. **Life-long learning**: Ability to analyze individual needs and engage in updating in the context of context of technological changes.

Semester V	**VLSI (Course Code:4350302)**						
	POs						
Competency & Course Outcomes	PO 1 Basic & Discipline specific knowledge	PO 2 Problem Analysis	PO 3 Design / development of solutions	PO 4 Engineering Tools, Experimentation &Testing	PO 5 Engineering practices for society, sustainability & environment	PO 6 Project Management	PO 7 Life-long learning
Competency	**Develop Verilog programs for VLSI based electronic systems**						
Course Outcomes CO1 Describe working of MOSFET system.	3	1	1	1	-	-	2

CO2 Maintain MOS inverters	2	3	1	2	-	-	2
CO3 Maintain MOS circuits	3	3	3	2	2	2	2
CO4 Describe fabrication process for MOS	3	2	2	3	3	2	3
CO5 Develop VERILOG Programs for combinational and sequential circuits	2	3	3	3	3	3	2

*Legend: '**3**' for high, '**2**' for medium, '**1**' for low and '**-**' for no correlation of each CO with PO.*

16. COURSE CURRICULUM DEVELOPMENT COMMITTEE

GTU Resource Persons

Sr. No.	Name and Designation	Institute	Contact No.	Email
1.	Prof. N M Rindani	AVPTI, Rajkot	9898533198	nmrindani@gmail.com
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