

GUJARAT TECHNOLOGICAL UNIVERSITY (GTU)

Competency-focused Outcome-based Green Curriculum-2021 (COGC-2021)

Semester-III

Course Title: Fundamentals of Digital Electronics

(Course Code: 4330303)

Diploma programme in which this course is offered	Semester in which offered
Biomedical Engineering	Third

1. RATIONALE

The objective of Fundamental of Digital Electronics is to make the students understand functioning of adigital circuit. The course contains description of digital components using core structure of digital logic.This includes number system, Logic gates, Boolean algebra, Combinational logic. This Course willenable student to solve various Boolean expressions, to design and implement digital logic circuits.

2. COMPETENCY

The course content should be taught and implemented with the aim to develop different types of skillsleading to the achievement of the following competencies.

- Design sequential and combinational circuits of any electronic device.

3. COURSE OUTCOMES (COs)

The practicalexercises, the underpinning knowledgeand the relevant soft skills associated with this competency are to be developed in the student to display the following COs:

- 1. Perform the conversion among different types of number systems.**
- 2. Apply Boolean laws to simplify digital circuits.**
- 3. Test different types of combinational logic circuits.**
- 4. Test different types of sequential logic circuits.**
- 5. Illustrate the working of flip flops.**

4. TEACHING AND EXAMINATION SCHEME

Teaching Scheme (In Hours)			Total Credits (L+T+P/2)	Examination Scheme				Total Marks
L	T	P		Theory Marks		Practical Marks		
			C	CA	ESE	CA	ESE	
3	0	2	5	30	70	25	25	150

():Out of 30 marks under the theory CA, 10 marks are for assessment of the micro-project to facilitate integration of COs and the remaining 20 marks is the average of 2 tests to be taken during the semester for the assessing the attainment of the cognitive domain UOs required for the attainment of the COs.*

Legends: *L-Lecture; T – Tutorial/Teacher Guided Theory Practice; P -Practical; C – Credit, CA - Continuous Assessment; ESE -End Semester Examination.*

5. SUGGESTED PRACTICAL EXERCISES

The following practical outcomes (PrOs) that are the sub-components of the COs. Some of the PrOs marked "*" are compulsory, as they are crucial for that particular CO at the 'Precision Level' of Dave's Taxonomy related to 'Psychomotor Domain'.

S. No.	Practical Outcomes (PrOs)	Unit No.	Approx. Hrs. required
1	Test the functionality of Basic Logic Gates.	2	2
2	Test the functionality of Advance Logic Gates.	2	2
3	Implement the basic logic gates using NAND Gate.	2	2
4	Implement the basic logic gates using NOR Gate.	2	2
5	Simplify and design Boolean expression using basic logic gates	2	2
6	Build/Test logic circuits for De Morgan's theorems.	2	2
7	Design and implement Half Adder and full adder circuit.	3	2
8	Design and implement Half Subtractor and full Subtractor circuit.	3	2
9	Design and implement Encoder and Decoder circuit	4	2
10	Design and implement Multiplexer and Demultiplexer circuit	4	2
11	Design and implement a circuit to Convert 4 bit Binary to Gray Code using logic gates.	3	2
12	Design and implement a circuit to Convert 4 bit Gray to Binary Code using logic gates.	3	2
13	Design and implement the functionality of the SR and D Flip-Flop.	5	2
14	Design and implement the functionality of the JK and T Flip-flops.	5	2
	Total		28

Note

- i. More **Practical Exercises** can be designed and offered by the respective course teacher to develop the industry relevant skills/outcomes to match the COs. The above table is only a suggestive list.
- ii. The following are some **sample** 'Process' and 'Product' related skills (more may be added/deleted depending on the course) that occur in the above listed **Practical Exercises** of this course required which are embedded in the COs and ultimately the competency..

S. No.	Sample Performance Indicators for the PrOs	Weightage in %
1	Design a simple digital circuit.	20
2	Prepare an experimental setup.	20
3	Operate the equipment setup or the circuit.	20

S. No.	Sample Performance Indicators for the PrOs	Weightage in %
4	Record observations correctly.	20
5	Interpret the results correctly and conclude.	20
Total		100

6. MAJOR EQUIPMENT/ INSTRUMENTS REQUIRED

This major equipment with broad specifications for the PrOs is a guide to procure them by the administrators to usher in uniformity of practicals in all institutions across the state.

S. No.	Equipment Name with Broad Specifications	PrO.No.
1	Variable DC regulated power supply 0-30V	All
2	Basic Logic Gates using Diode & Transistor	1,2
3	AND, OR, NOT Gate Characteristics kit	1,2
4	NAND, NOR, EX-OR Gate Characteristics kit	1,2,3,4
5	NAND & NOR as Universal Gate Trainer Kit	3,4
6	Half & Full Adder Trainer Kit	7
7	Half & Full Subtractor Trainer Kit	8
8	Binary to Gray code Converter & Gray to Binary code Converter	11,12
9	Decoder and Encoder Trainer Kit	9
10	Multiplexer / De-multiplexer Trainer Kit	10
11	Flip-Flop Trainer Kit	12,13
12	Bread Board Trainer (For Digital IC's)	All

7. AFFECTIVE DOMAIN OUTCOMES

The following *sample* Affective Domain Outcomes (ADOs) are embedded in many of the above mentioned COs and PrOs. More could be added to fulfil the development of this competency.

- a) Work as a leader/a team member.
- b) Follow safety practices while using electrical and electronic equipment.
- c) Practice environmental friendly methods and processes. (Environment related)

The ADOs are best developed through the laboratory/field based exercises. Moreover, the level of achievement of the ADOs according to Krathwohl's 'Affective Domain Taxonomy' should gradually increase as planned below:

- i. 'Valuing Level' in 1st year
- ii. 'Organization Level' in 2nd year.
- iii. 'Characterization Level' in 3rd year.

8. UNDERPINNING THEORY

Only the major Underpinning Theory is formulated as higher level UOs of *Revised Bloom's taxonomy* in order development of the COs and competency is not missed out by the students and teachers. If required, more such higher level UOs could be included by the course teacher to focus on attainment of COs and competency.

Unit	Unit Outcomes (UOs) (4 to 6 UOs at Application and above level)	Topics and Sub-topics
Unit – I Introduction to Digital Circuits and Number Systems	1a. Introduction to Digital Circuits 1b. Types of Number Systems 1c. Inter-conversions between number systems 1d. Binary Codes	1.1 Fundamentals of Analog and Digital Circuits. 1.2 Comparison between Analog and Digital Circuits. 1.3 Number Systems: Binary, Octal and Hexadecimal 1.4 Number Base Conversions. 1.5 Complements: r 's and $(r-1)$'s complements 1.6 BCD, Excess-3, Error detection, Gray code.
Unit – II Binary Logic And Boolean algebra	2a. Concept of Binary Logic 2b. Logic Gates 2c. Introduction to Boolean algebra 2d. Boolean expression implementation using logic gates 2e. Solve Boolean expression 2f. Boolean function simplification	2.1 Concept of Positive and Negative logic. 2.2 Operation, symbol and truth table of various logic gates. 2.3 Basic definitions, theorems and postulates of Boolean algebra. 2.4 Boolean Functions. 2.5 Canonical and Standard forms. 2.6 Boolean function implementation using logic gates. 2.7 Boolean function simplification using Karnaugh Map: Two, three and four variable K-Map. 2.8 SOP and POS Simplification.
Unit– III Basic Combinational Logic	3a. Basics of Combinational Logic 3b. Adders and Subtractors 3c. Code Conversion	3.1 Introduction to combinational logic. 3.2 Design procedure for combinational circuits. 3.3 Design of Half Adders, Full Adders, Half Subtractors and Full Subtractors. 3.4 BCD to Excess-3 code convertor.

Unit– IV Combinational Logic with MSI, LSI	4a. Combinational circuits with MSI and LSI 4b. Encoders and Decoders 4c. Multiplexers and Demultiplexers	4.1 Design of Binary Parallel adder, BCD adder and Magnitude comparator. 4.2 Concept of Encoders and Decoders. 4.3 Concept of Multiplexers and Demultiplexers.
Unit– V Basic Sequential Circuits	5a. Difference between combinational and sequential circuits 5b. Types of Flip-flops 5c. Basics of Counters	5.1 Introduction to sequential circuits. 5.2 Theory, logic diagram and truth table of various types of flip-flops, 5.3 Theory and application of Counters in digital circuits.

Note: The UOs need to be formulated at the 'Application Level' and above of Revised Bloom's Taxonomy' to accelerate the attainment of the COs and the competency.

9. SUGGESTED SPECIFICATION TABLE FOR QUESTIONPAPER DESIGN

Unit No.	Unit Title	Teaching Hours	Distribution of Theory Marks			
			R Level	U Level	A	Total Marks
I	Introduction to Digital Circuits and Number Systems	8	8	4	3	15
II	Binary Logic and Boolean algebra	10	4	5	6	15
III	Basic Combinational Logic	8	4	5	6	15
IV	Combinational Logic with MSI, LSI	8	6	4	5	15
V	Basic Sequential Circuits	8	4	2	4	10
Total		42	26	20	24	70

Legends: R=Remember, U=Understand, A=Apply and above (Revised Bloom's taxonomy)

Note: This specification table provides general guidelines to assist student for their learning and to teachers to teach and question paper designers/setters to formulate test items/questions assess the attainment of the UOs. The actual distribution of marks at different taxonomy levels (of R, U and A) in the question paper may vary slightly from above table.

10. SUGGESTED STUDENT ACTIVITIES

Other than the classroom and laboratory learning, following are the suggested student-related **co-curricular** activities which can be undertaken to accelerate the attainment of the various outcomes in this course: Students should conduct following activities in group and prepare reports of about 5 pages for each activity, also collect/record physical evidences for their (student's) portfolio which will be useful for their placement interviews:

- Prepare a chart/poster demonstrating different types of logic gates with its logic diagram, symbol and truth table.

- b) Seminar on various types of IC digital logic families.
- c) Seminar on types of counters highlighting their common applications.

11. SUGGESTED SPECIAL INSTRUCTIONAL STRATEGIES (if any)

These are sample strategies, which the teacher can use to accelerate the attainment of the various outcomes in this course:

- a) Massive open online courses (**MOOCs**) may be used to teach various topics/sub topics.
- b) Guide student(s) in undertaking micro-projects.
- c) '**L**' in **section No. 4** means different types of teaching methods that are to be employed by teachers to develop the outcomes.
- d) About **20% of the topics/sub-topics** which are relatively simpler or descriptive in nature is to be given to the students for **self-learning**, but to be assessed using different assessment methods.
- e) With respect to **section No.10**, teachers need to ensure to create opportunities and provisions for **co-curricular activities**.
- f) Guide students on how identify and utilize Integrated circuits for simple applications.
- g) Guide students for using data manuals.

12. SUGGESTED LEARNING RESOURCES

S. No.	Title of Book	Author	Publication with place, year and ISBN
1	Digital Logic and Computer Design	Morris Mano	Pearson Publication, 2004 ISBN 10: 817758409X ISBN 13: 978-8177584097
2	Digital Principles and Applications	Donald P Leach Albert Paul Malvino	Tata McGraw-Hills publication, 2014 ISBN 10: 9789339203405 ISBN-13: 978-9339203405
3	Modern Digital Electronics	Jain R.P	Tata McGraw-Hills publication, 2009 ISBN 10: 0070669112 ISBN 13: 978-0070669116
4	Fundamentals of Digital Circuits.	Anand Kumar	Prentice-Hall of India, 2016 ISBN 10: 8120352688 ISBN 13: 978-8120352681

13. SOFTWARE/LEARNING WEBSITES

- a. www.nptel.iitm.ac.in
- b. www.khanacademy.org
- c. <https://phet.colorado.edu/>
- d. <https://ndl.iitkgp.ac.in>
- e. www.electrical4u.com
- f. www.vlab.co.in

14. PO-COMPETENCY-CO MAPPING

Semester I	FDE (Course Code: 4330303)						
	POs						
Competency & Course Outcomes	PO 1 Basic & Discipline specific knowledge	PO 2 Problem Analysis	PO 3 Design/ development of solutions	PO 4 Engineering Tools, Experimentation & Testing	PO 5 Engineering practices for society, sustainability & environment	PO 6 Project Management	PO 7 Life-long learning
Competency "Solve basic circuit problems using circuit laws and network theorems."							
CO a) Perform the conversion among different types of number systems	2	1	1	-	-	-	1
CO b) Apply Boolean laws to simplify digital circuits.	2	2	2	-	-	-	1
CO c) Test different types of combinational logic circuits.	2	3	2	2	-	-	1
CO d) Test different types of sequential logic circuits.	2	3	2	2	-	-	1
CO e) Illustrate the working of flip flops.	1	-	1	2	-	-	1

Legend: '3' for high, '2' for medium, '1' for low or '-' for the relevant correlation of each competency, CO, with PO/ PSO

15. COURSE CURRICULUM DEVELOPMENT COMMITTEE

GTU Resource Persons

S. No.	Name and Designation	Institute	Contact No.	Email
1	V.D.Parmar, Lecturer	GP, Ahmedabad	8511562348	viralparmar.bme@gmail.com
2	K.H.Parmar, Lecturer	AVPTI, Rajkot	9377628856	krunal.parmar03@gmail.com
3	H.V.Rupala, Lecturer	GP, Gandhinagar	9099952581	rupala229@gmail.com
4	N.B.Modi, Lecturer	GGP, Ahmedabad	9265538994	neelambm21@gmail.com