BASIC ELECTRONICS [3320701]

– THE TRANSISTORS

TRANSISTOR

- History:-

In 1906, an American Inventor and Physicist, Lee De Forest, made the vacuum tube triode as he called it.

Used in Radios,

Used in early computers.

Transistor

WHAT IS A TRANSISTOR?

- When an N-type or P-type semiconductor is connect between two P-type or N-type semiconductor respectively then two PN Junction formed. Such a two junction device is called as TRANSISTOR.

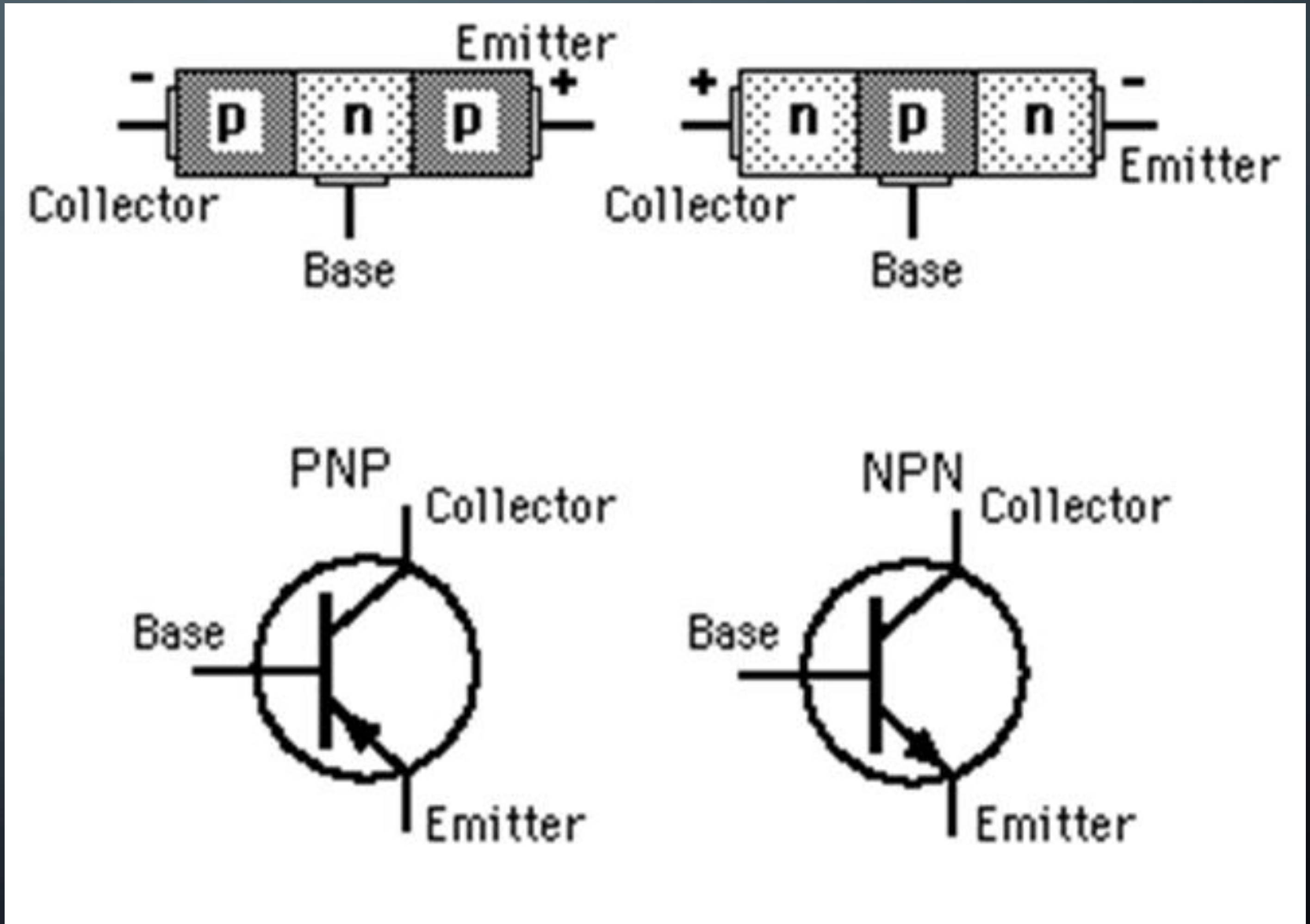
- Thus it is a two junction, three layered, three terminal semiconductor device. It is made by Silicon or Germanium material.

- Transistor has mainly 2 types:-

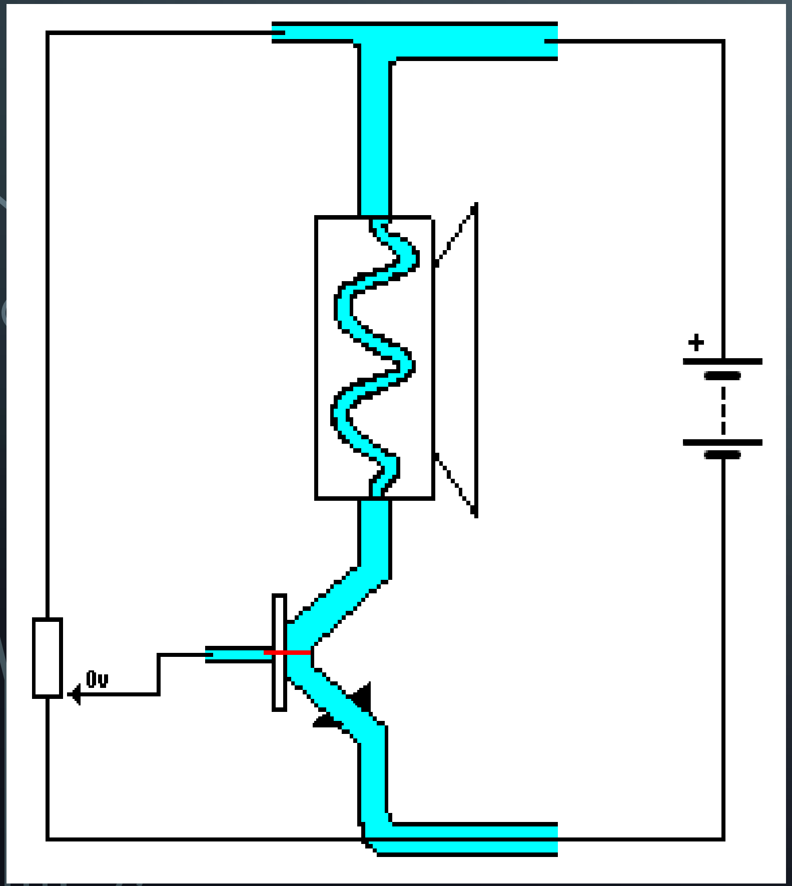
  1. PNP Transistor
  2. NPN Transistor

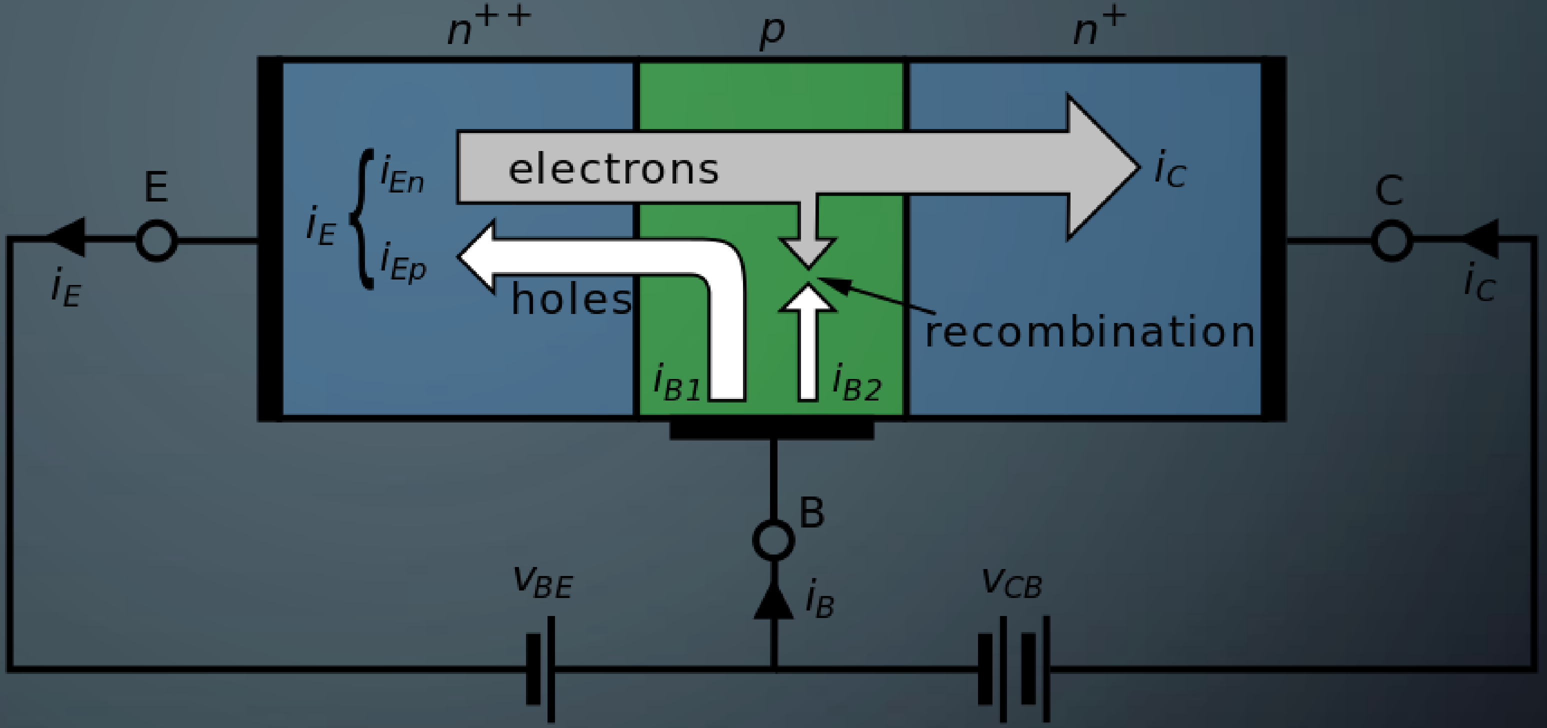
WHAT IS A TRANSISTOR?

Transistor Symbol:-



TRANSISTOR OPERATION

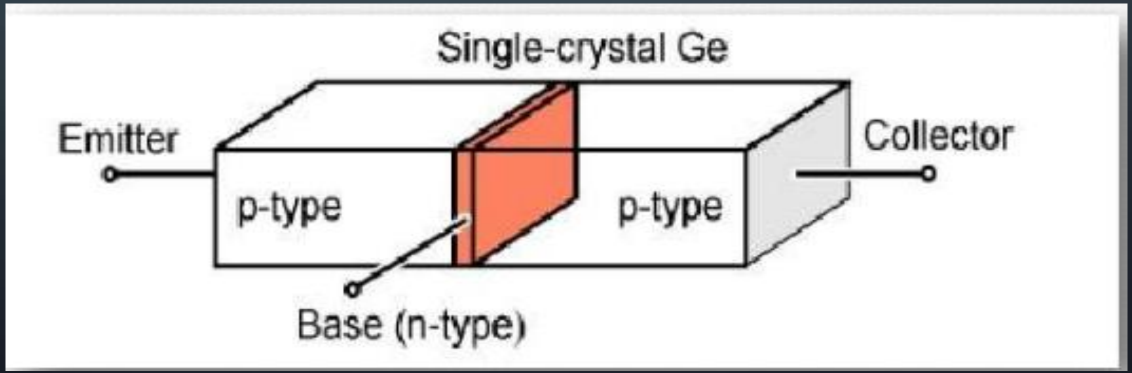




REGIONS OF A TRANSISTOR

- A Transistor has 3 regions namely:-

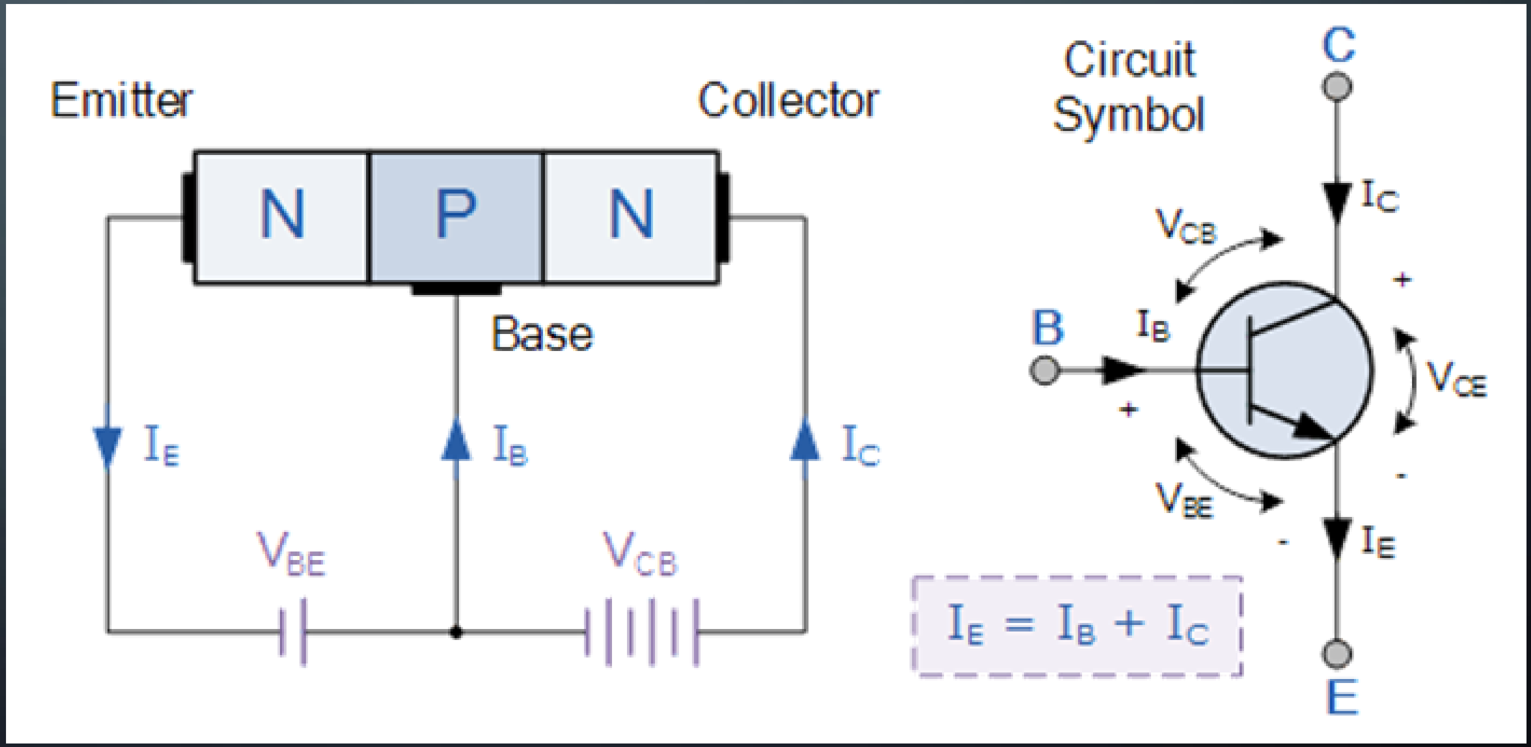
1) Emitter → heavily doped → larger than Base.
2) Base → lightly doped → Thin.
3) Collector → moderately doped → larger than Emitter.



BIASING ARRANGEMENT OF TRANSISTOR.

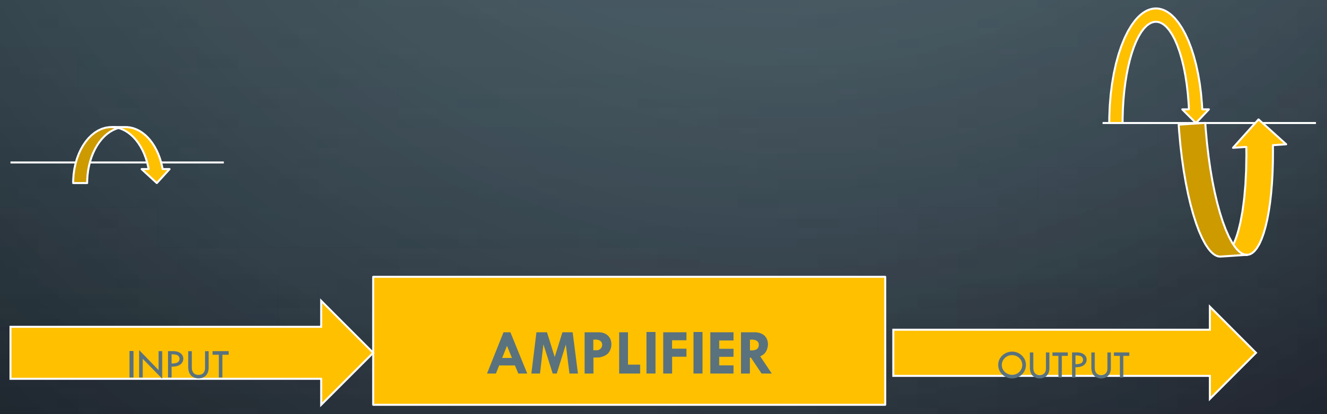
- The Base – Emitter(BE) junction is Forward biased.
- The Base – Collector(BC) junction is Reverse biased.

- $I_E = I_B + I_C$



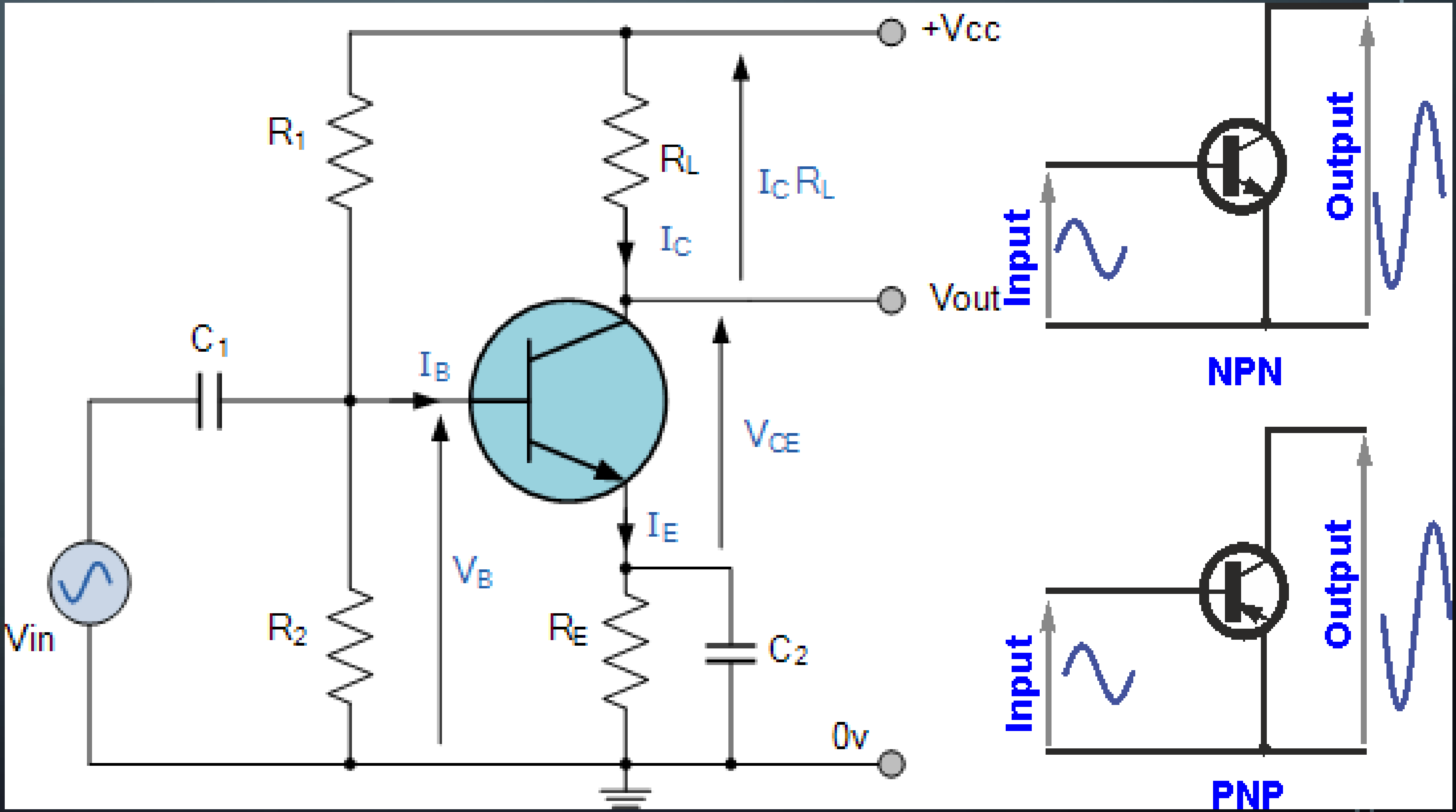
AMPLIFIER

- The device which converts low magnitude signal into the signal of higher magnitude is called the amplifier and this process of converting the signal of low magnitude in to higher magnitude is called amplification.



COMMON EMITTER AMPLIFIER

- Due to the small changes in base current, the collector current will mimic with greater amplitude.



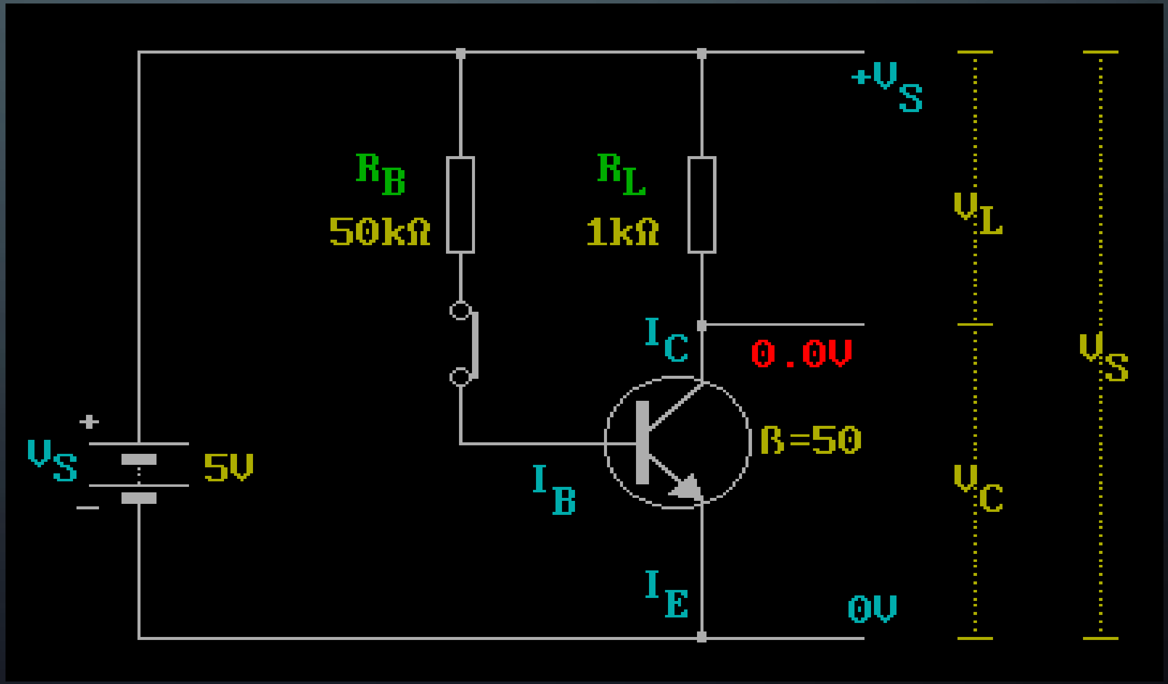
PARAMETERS:

	DC gains	AC gains
Voltage	$A_V = \frac{V_{output}}{V_{input}}$	$A_V = \frac{\Delta V_{output}}{\Delta V_{input}}$
Current	$A_I = \frac{I_{output}}{I_{input}}$	$A_I = \frac{\Delta I_{output}}{\Delta I_{input}}$
Power	$A_P = \frac{P_{output}}{P_{input}}$	$A_P = \frac{(\Delta V_{output})(\Delta I_{output})}{(\Delta V_{input})(\Delta I_{input})}$
	$A_P = (A_V)(A_I)$	

Δ = *"change in . . ."*

TRANSISTOR AS A SWITCH.

- NPN **Transistor as a Switch**. Based on the voltage applied at the base terminal of a **transistor switching** operation is performed. When a sufficient voltage (V_{in}> 0.7 V) is applied between the base and emitter, collector to emitter voltage is approximately equal to 0. Therefore, the **transistor** acts as a short circuit.



APPLICATION OF TRANSISTOR.

1. As small signal amplifier.

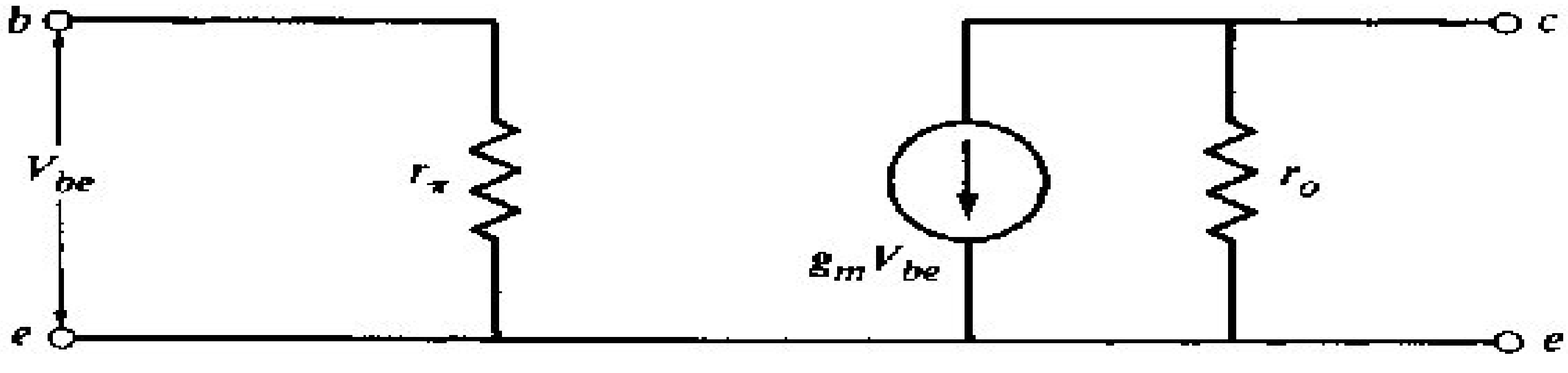
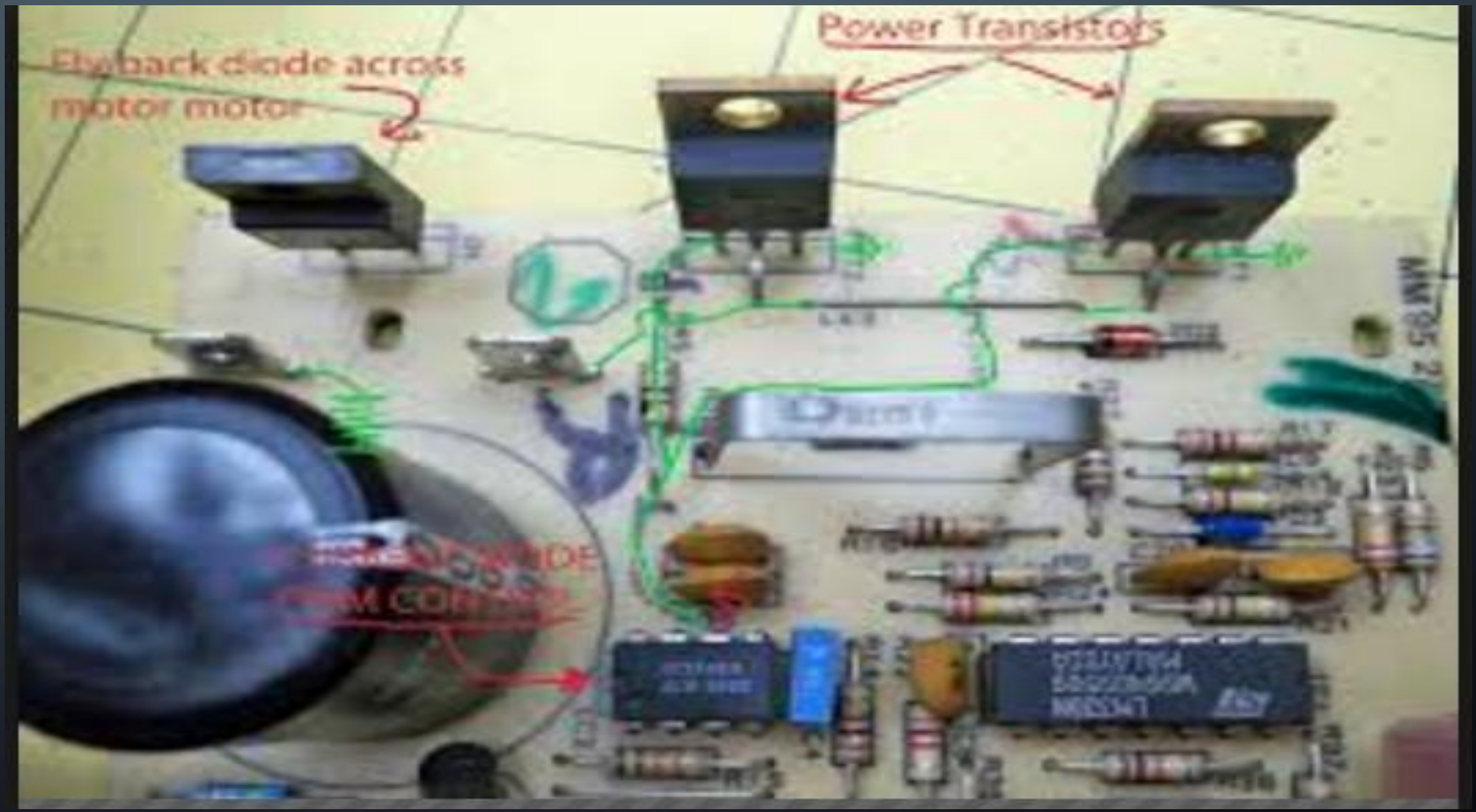


FIGURE 2.2
A simplified small-signal, midfrequency equivalent-circuit model of a bipolar transistor.

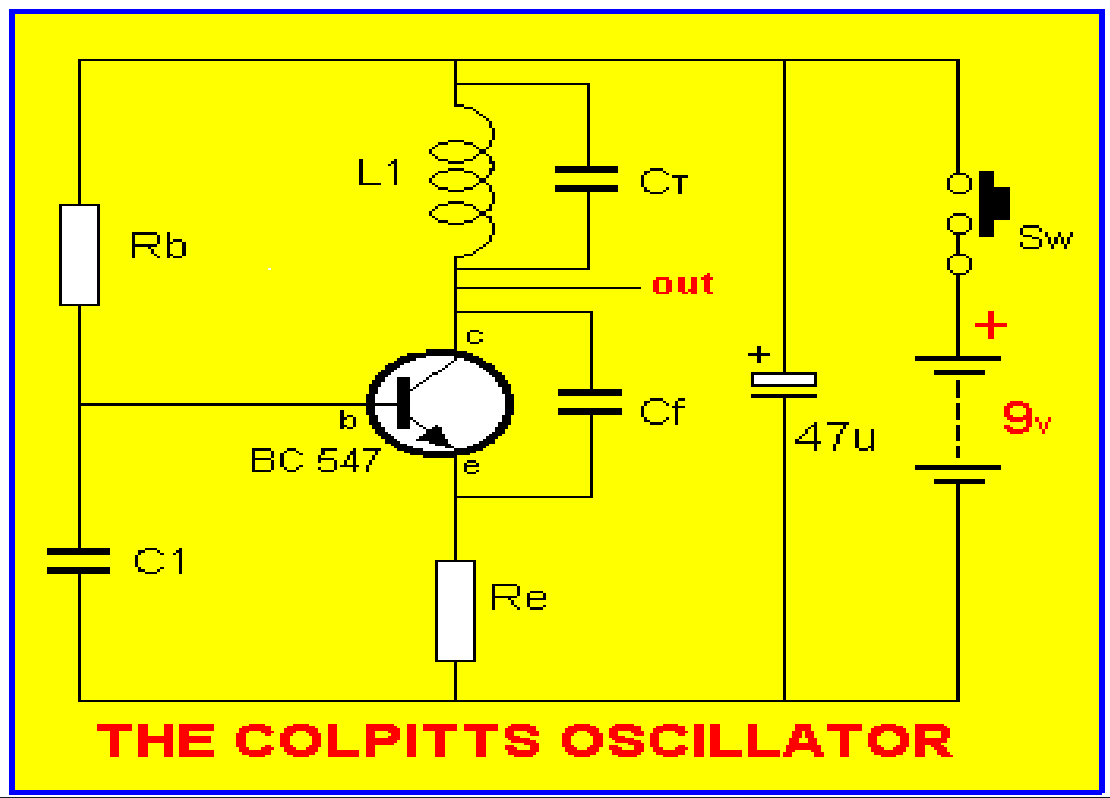
APPLICATION OF TRANSISTOR.

2. In Power Amplifier.



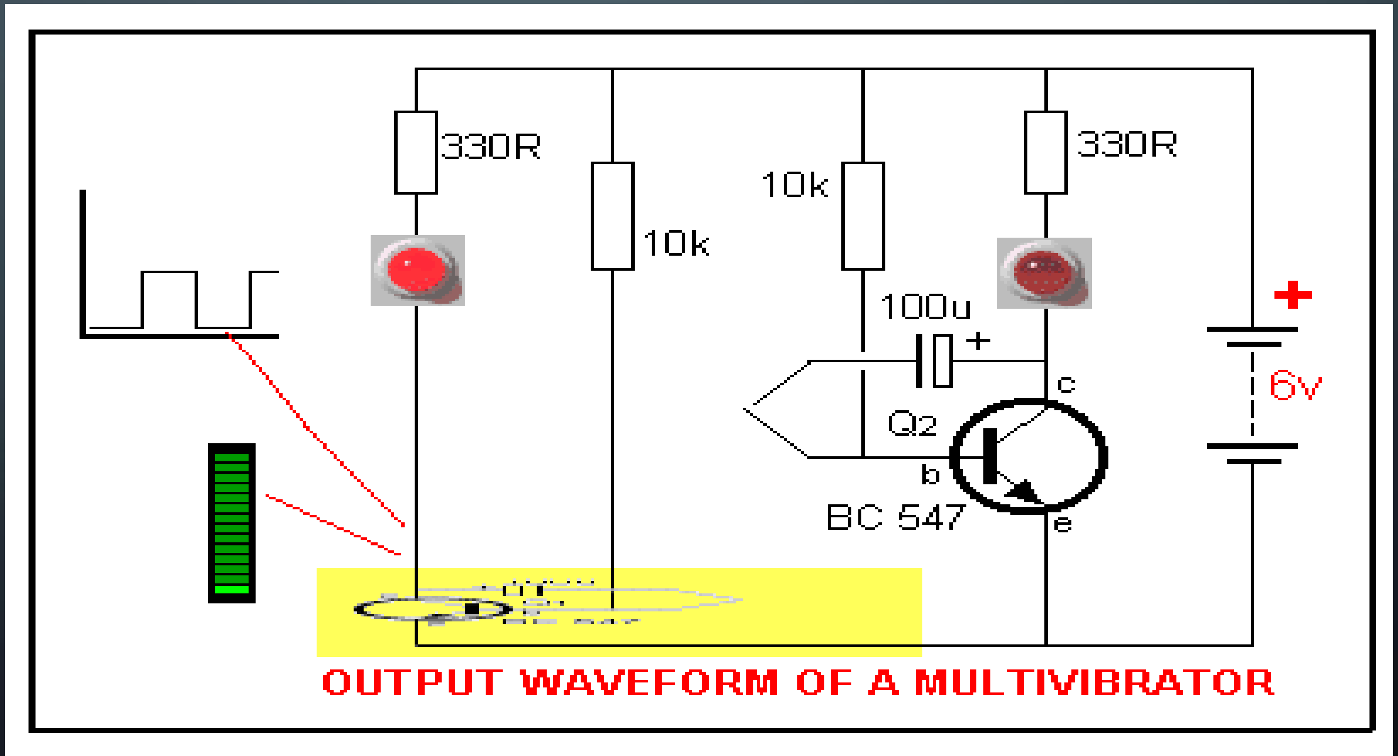
APPLICATION OF TRANSISTOR.

3. In Oscillator.



APPLICATION OF TRANSISTOR.

4. In Multivibrator.

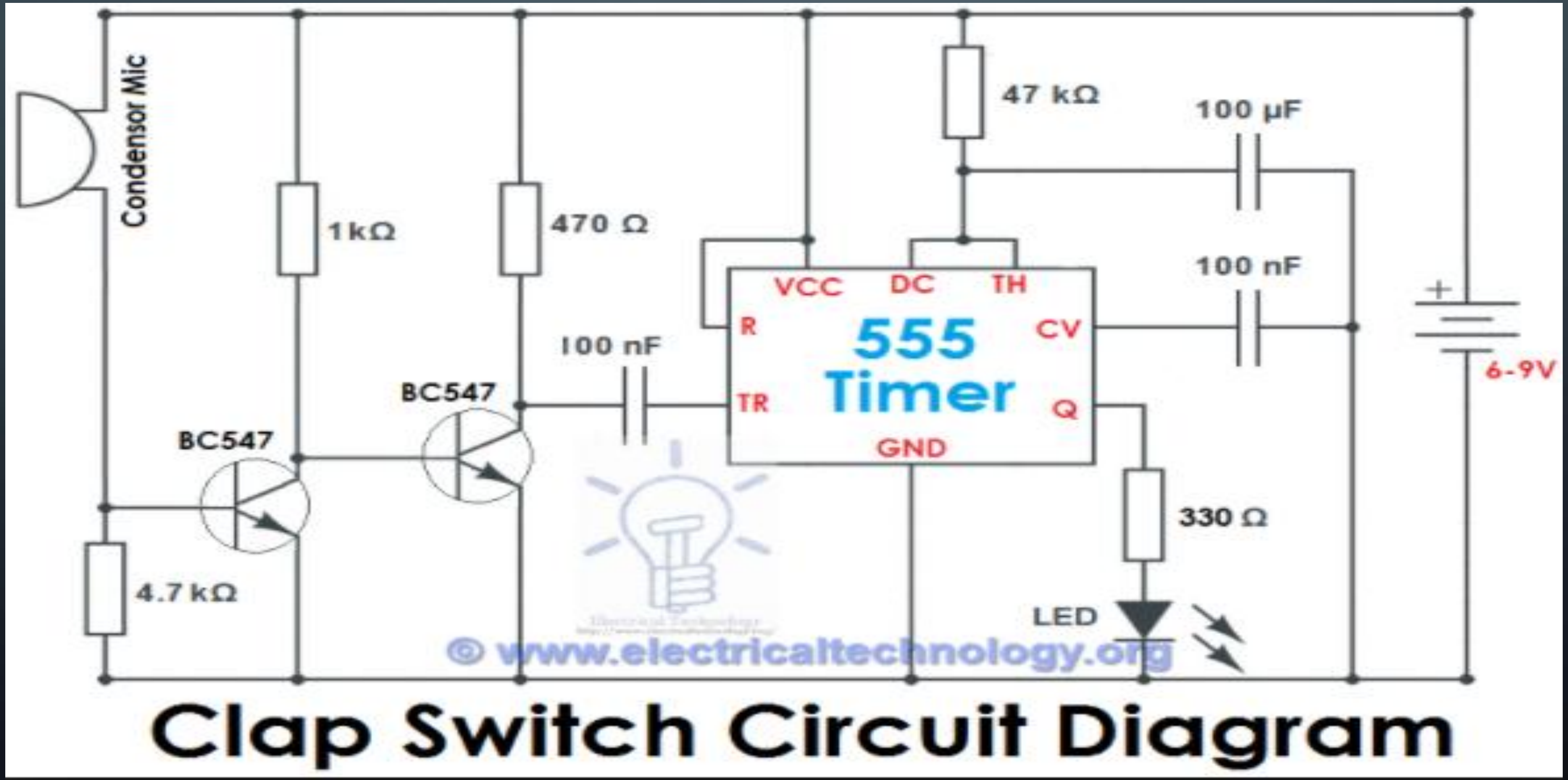


APPLICATION OF TRANSISTOR.

5. In Digital and Analog ICs.

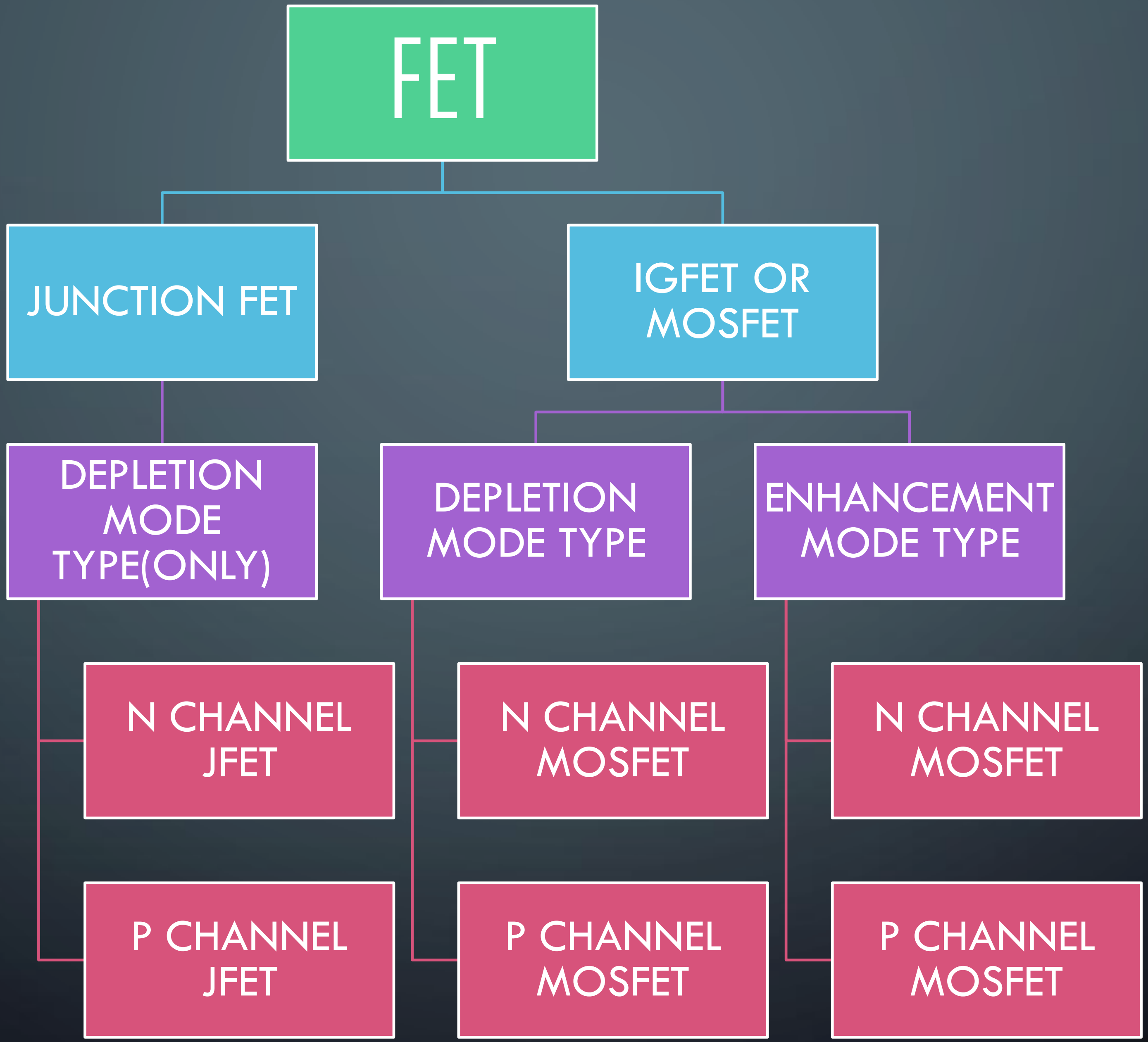
APPLICATION OF TRANSISTOR.

6. As Electronic Switch.

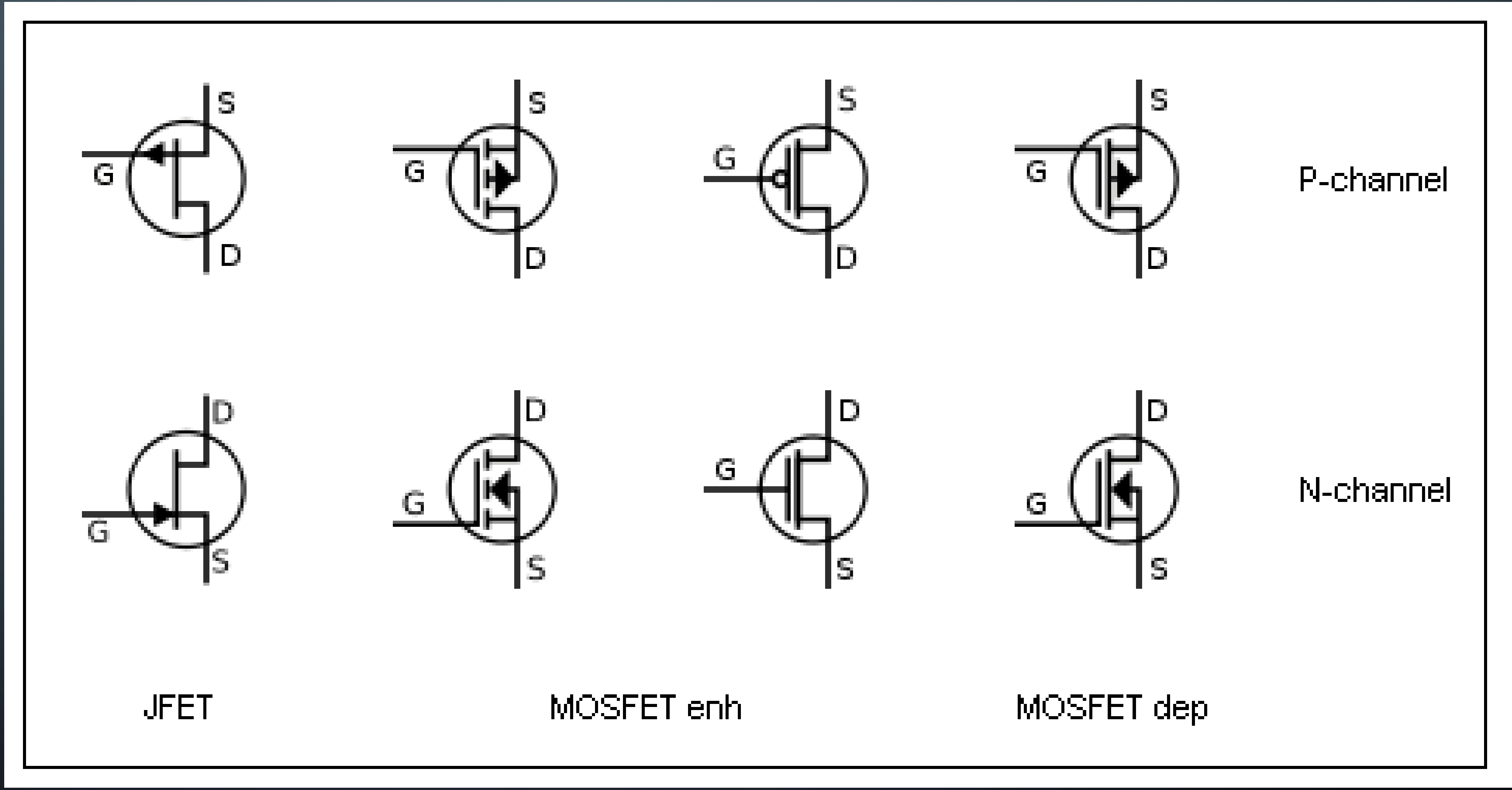


FET

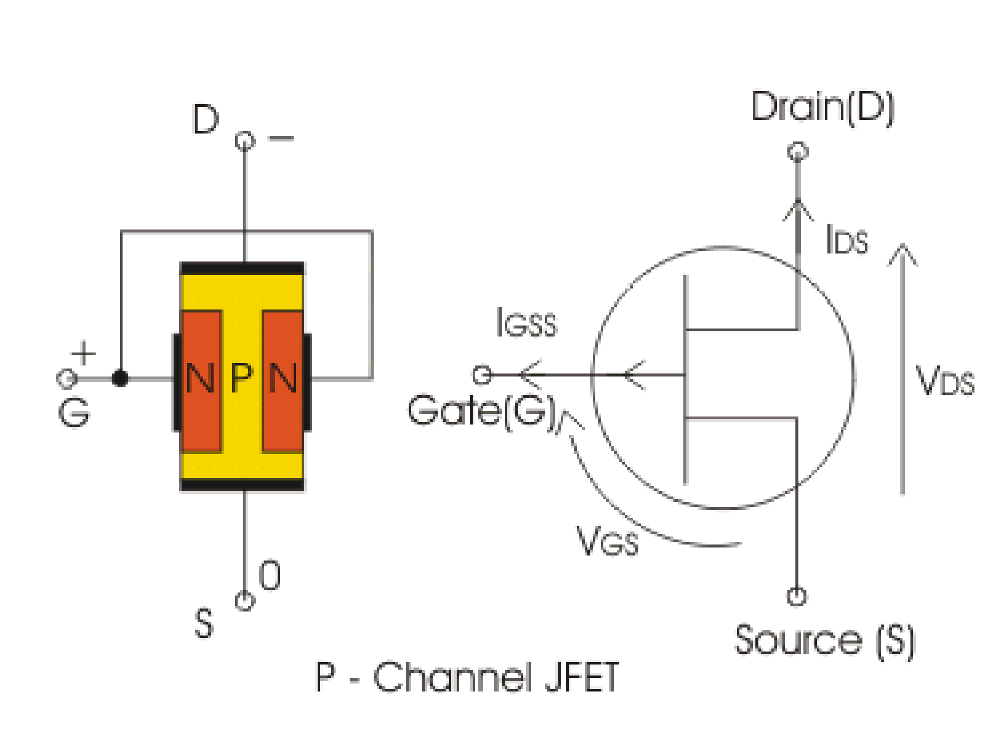
FIELD EFFECT TRANSISTOR

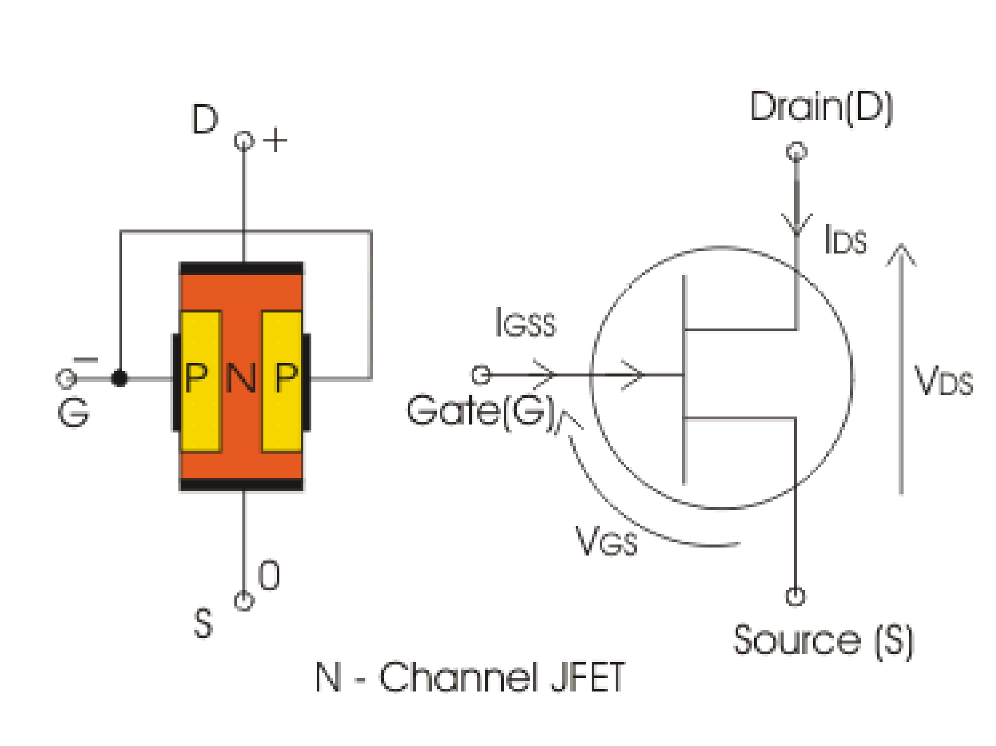

FET
JUNCTION FET
IGFET OR MOSFET
DEPLETION MODE TYPE(ONLY)
DEPLETION MODE TYPE
ENHANCEMENT MODE TYPE
N CHANNEL JFET
P CHANNEL JFET
N CHANNEL MOSFET
P CHANNEL MOSFET
N CHANNEL MOSFET
P CHANNEL MOSFET

FIELD EFFECT TRANSISTOR



P – CHANNEL & N – CHANNEL JUNCTION FIELD EFFECT TRANSISTOR





WORKING OF N – CHANNEL JFET

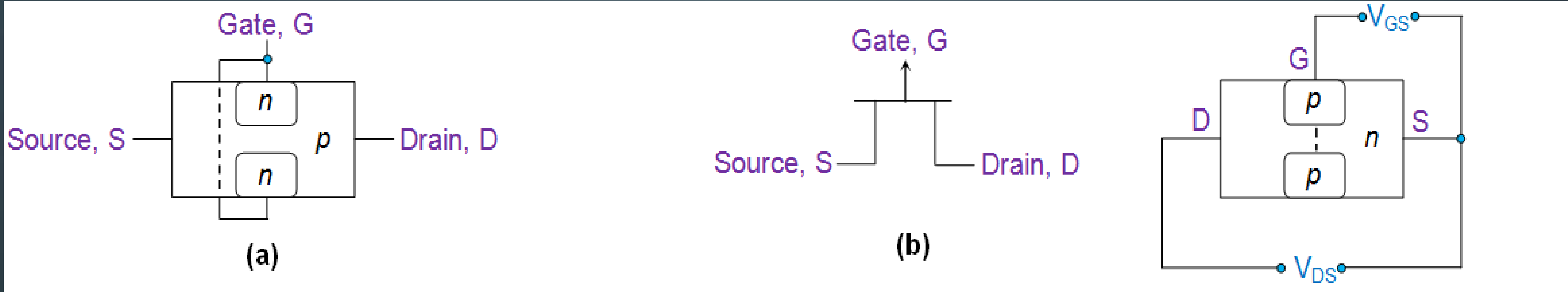


Figure 4 *p*-channel JFET **(a)** Layered Structure **(b)** Circuit Symbol

Figure 2 *n*-channel JFET in a Biased State

- In N-channel JFET, the majority charge carriers will be the electrons as the channel formed in-between the source and the drain is of n-type. Further, the working of these devices depends upon the voltages applied at its terminals.

WORKING OF P – CHANNEL JFET

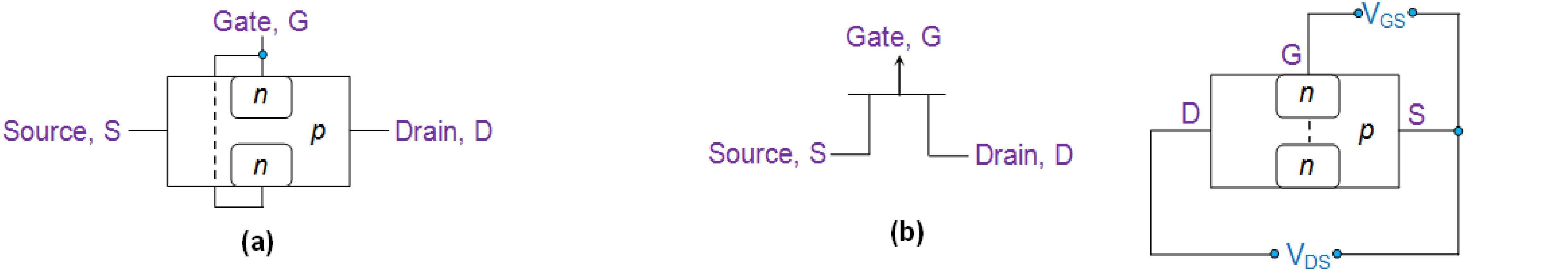


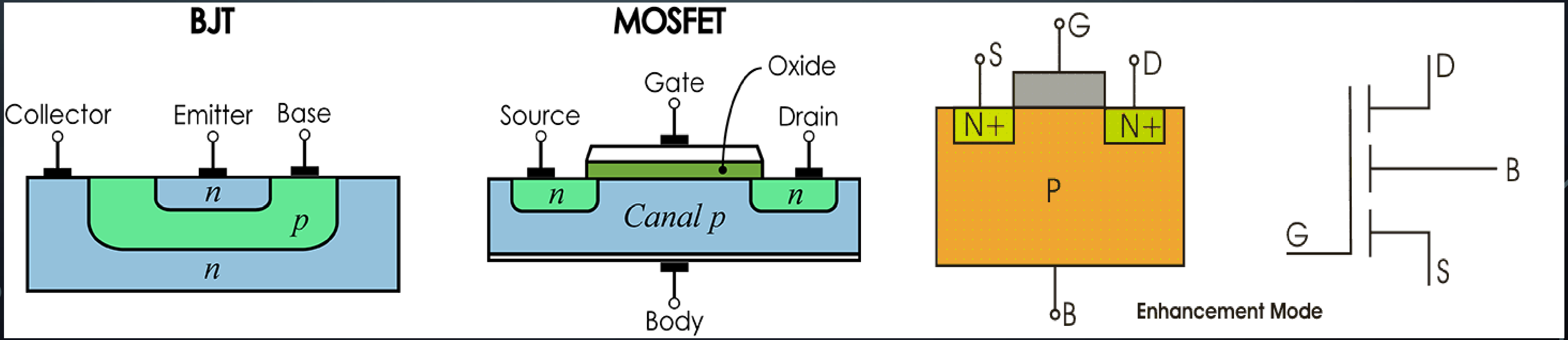
Figure 4 *p*-channel JFET **(a)** Layered Structure **(b)** Circuit Symbol

Figure 5 *p*-channel JFET in a Biased State

- Similar to the case of **N-channel JFETs**, the working of these devices also depends upon the voltages applied at its terminals.

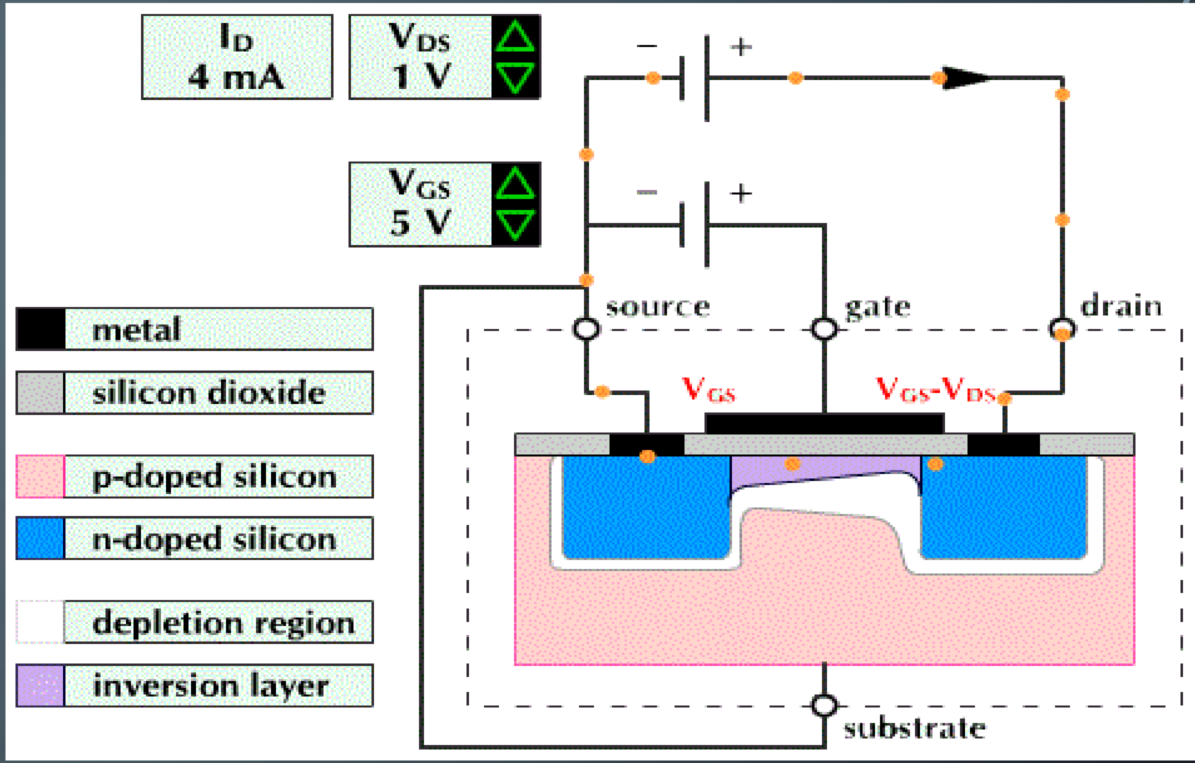
INSULATED GATE FET (IGFET) OR METAL OXIDE SEMICONDUCTOR FET (MOSFET)

- **MOSFET** having n-channel region between source and drain is known as **n-channel MOSFET** . It is a four terminal device, the terminals are gate, drain and source and substrate or body. The drain and source are heavily doped n+ region and the substrate is p-type. The current flows due to flow of the negatively charged electrons, that's why it is known as n- channel MOSFET.



WORKING OF N-CHANNEL ENHANCEMENT MODE INSULATED GATE FET:

- For the n-channel enhancement MOS transistor a drain current will only flow when a gate voltage (V_{GS}) is applied to the gate terminal greater than the threshold voltage (V_{TH}) level in which conductance takes place making it a trans conductance device.

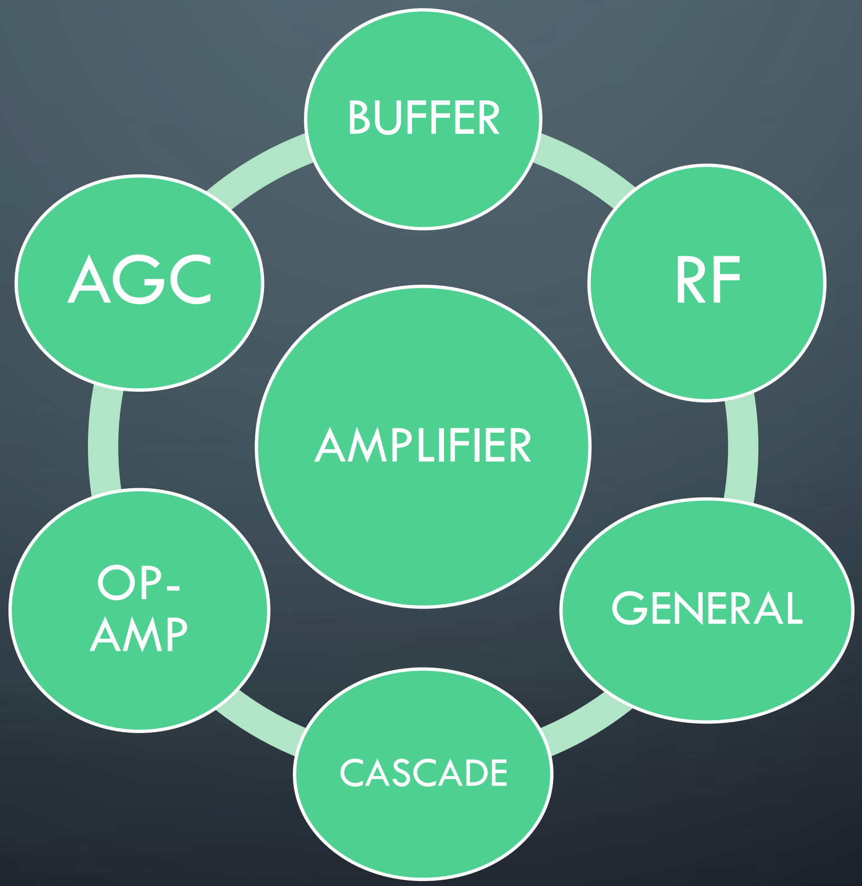


- The application of a positive (+ve) gate voltage to a n-type eMOSFET attracts more electrons towards the oxide layer around the gate thereby increasing or enhancing (hence its name) the thickness of the channel allowing more current to flow.

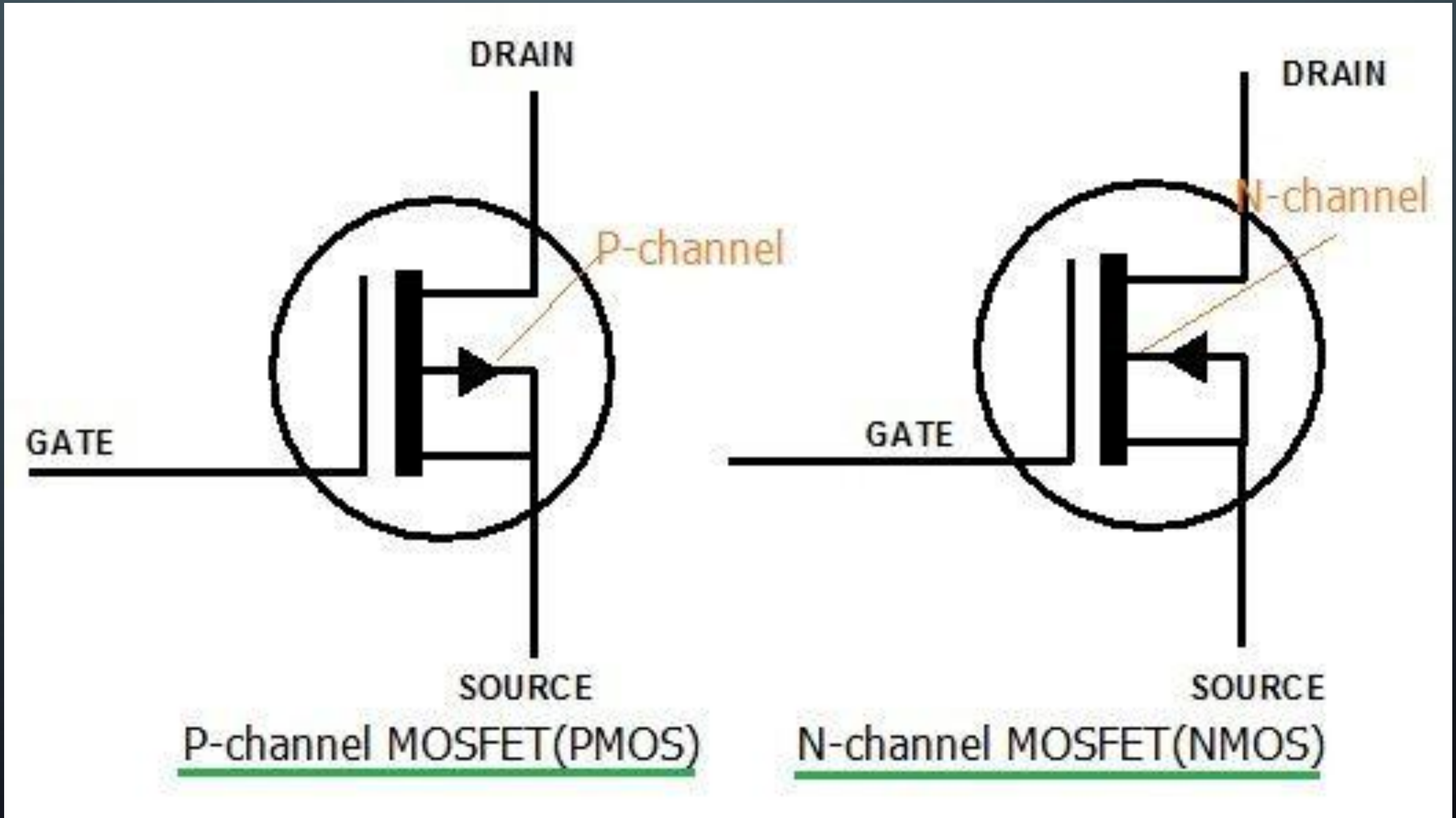
COMPARISON BETWEEN FET AND BJT

	JFET	BJT
1.	Unipolar device (current conduction is only due to one type of majority carrier either electron or hole).	Bipolar device (current condition, by both types of carriers, i.e., majority and minority- electrons and holes)
2.	The operation depends on the control of a junction depletion width under reverse bias.	The operation depends on the injection of minority carriers across a forward biased junction.
3.	Voltage driven device. The current through the two terminals is controlled by a voltage at the third terminal (gate).	Current driven device. The current through the two terminals is controlled by a current at the third terminal (base).
4.	Low noise level.	High noise level.
5.	High input impedance (due to reverse bias).	Low input impedance (due to forward bias).
6.	Gain is characterised by transconductance.	Gain is characterized by voltage gain.
7.	Better thermal stability.	Less thermal stability.

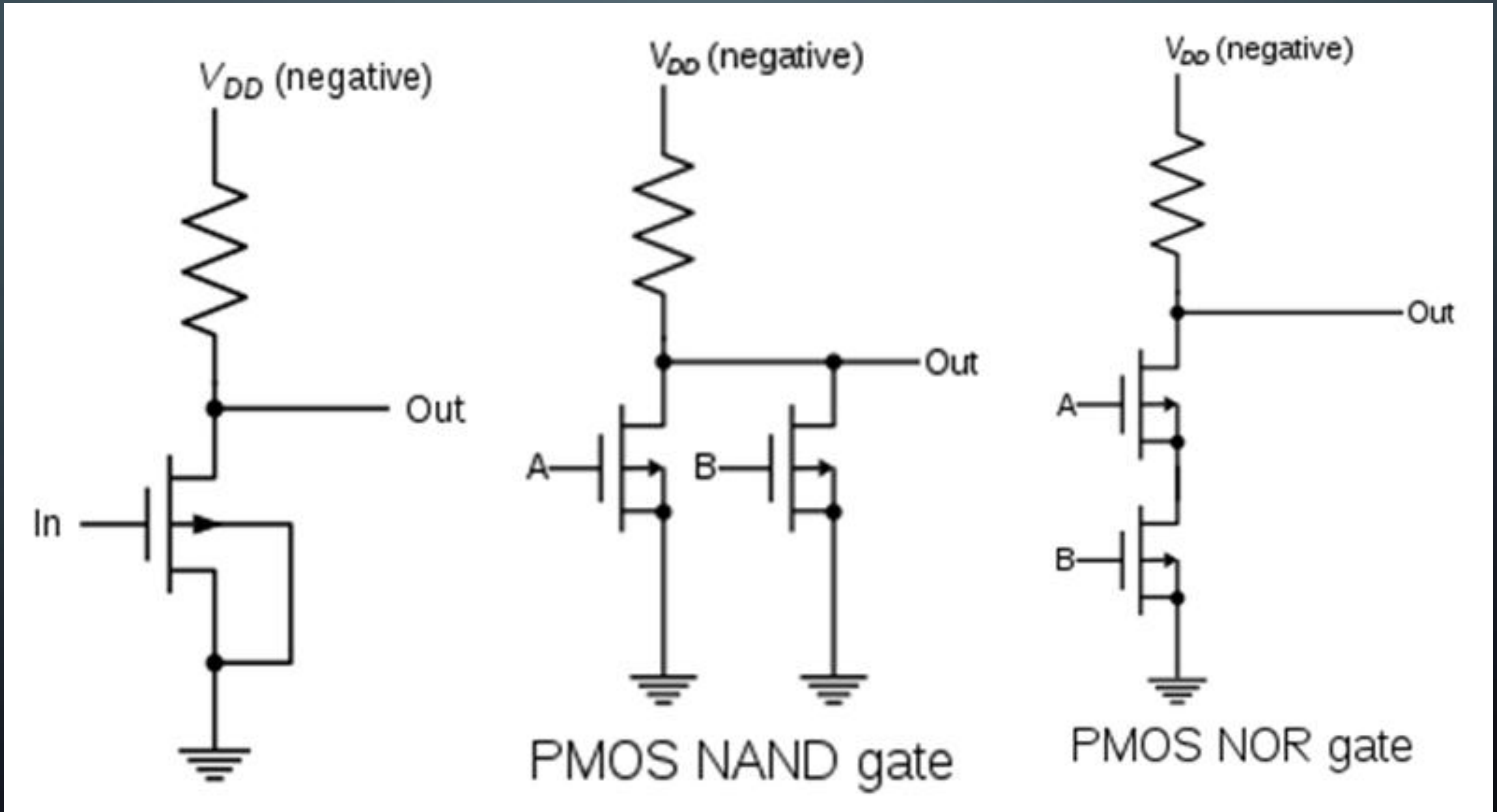
SOME APPLICATIONS OF FET:



MOS FAMILY

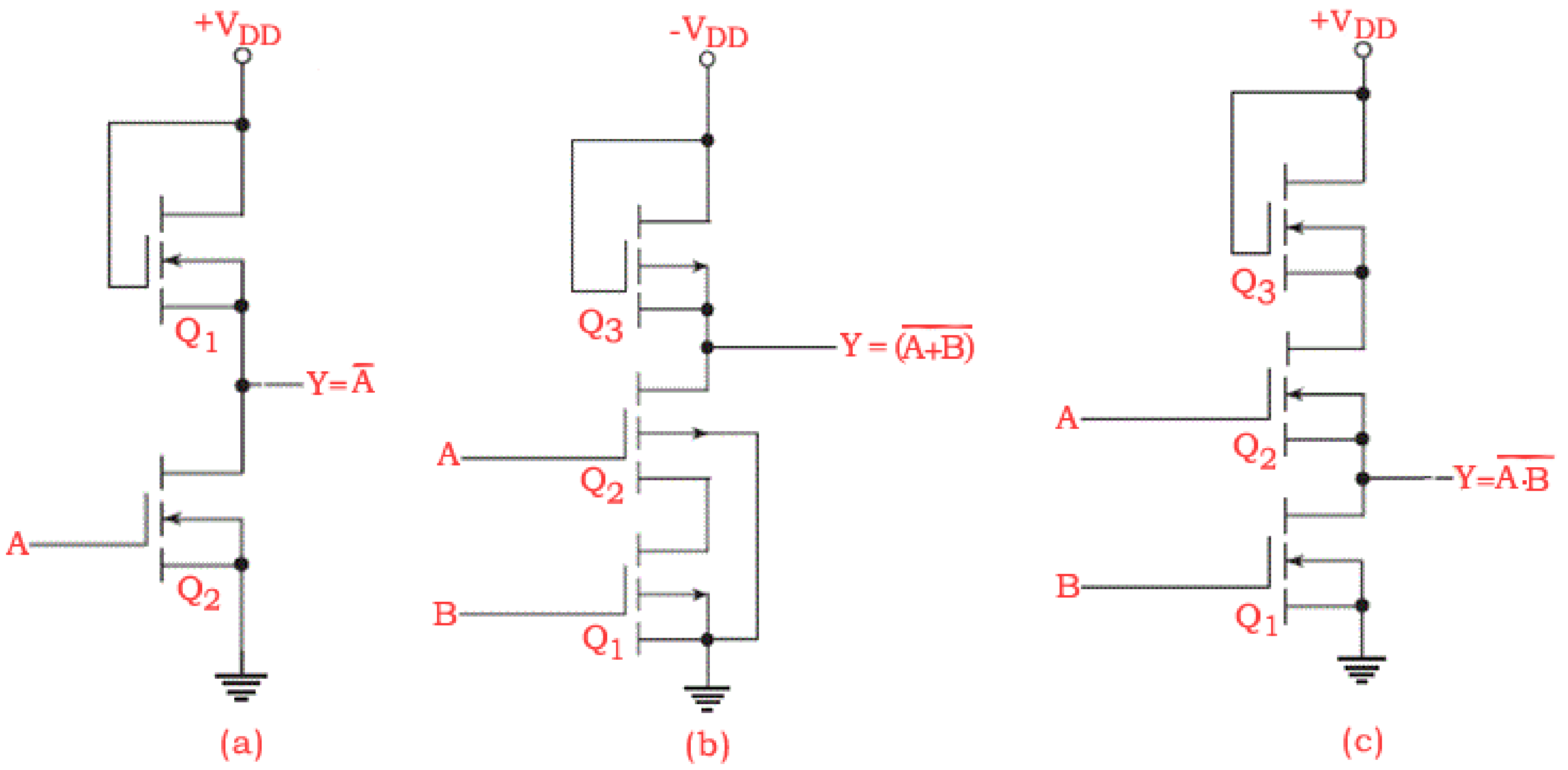

DRAIN
P-channel
GATE
SOURCE
P-channel MOSFET(PMOS)
DRAIN
N-channel
GATE
SOURCE
N-channel MOSFET(NMOS)

PMOS



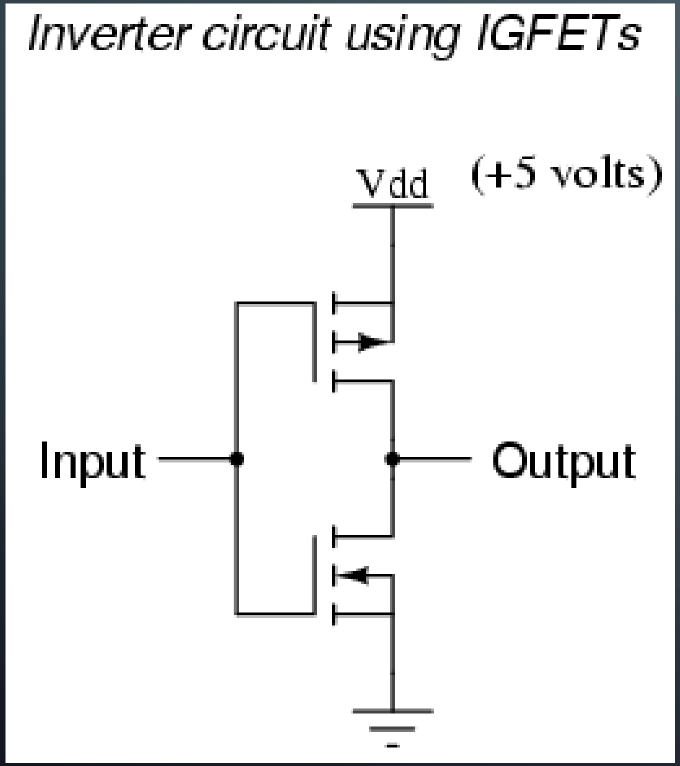
V_{DD} (negative)
Out
In
V_{DD} (negative)
Out
A
B
PMOS NAND gate
V_{DD} (negative)
Out
A
B
PMOS NOR gate

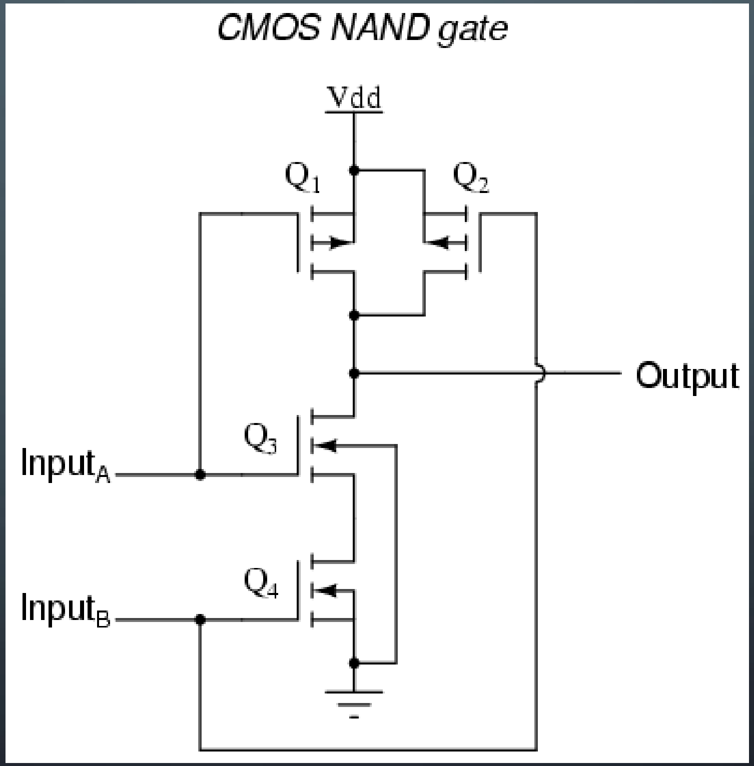
NMOS

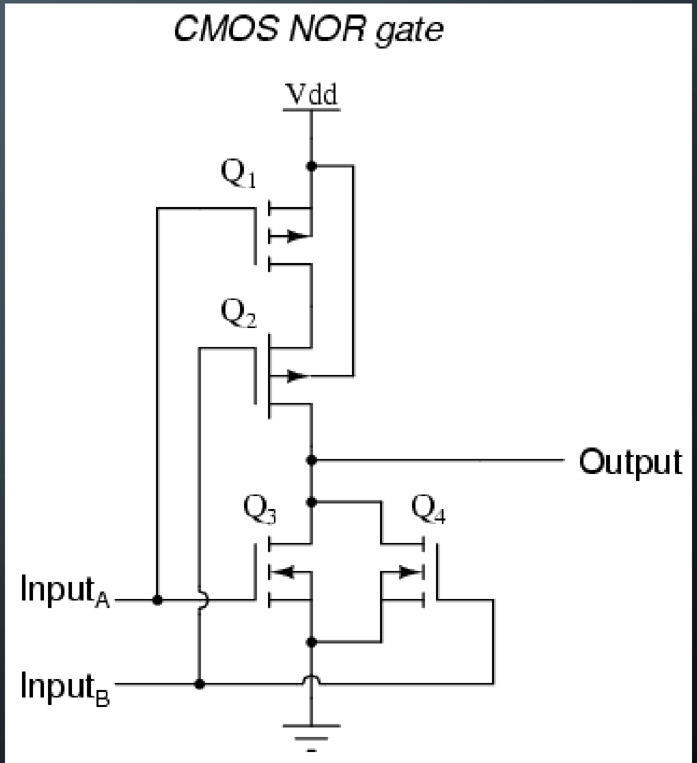


(a) NMOS logic circuit inverter, (b) NMOS logic two-input NOR
and
(c) NMOS logic two-input

COMPLEMENTARY MOSFET (CMOS)







ADVANTAGES OF CMOS ICS OVER TTL ICS:

- Negligible power dissipation.
- Simple Internal circuit.
- Less Power consumption.
- More Noise margin.
- Suitable for LSI and MSI.
- High fan out.

DISADVANTAGES OF CMOS ICS OVER TTL ICS:

- It should be stored in special conductive foam.
- Soldering iron should be earthed

  Or battery power supply should be used.
- More propagation time.
- Cost is more.

THANK YOU……